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TALLINN UNIVERSITY OF TECHNOLOGY

Dependable Embedded Systems: Design Implications of New and Scaled Technologies for Embedded Electronics and Systems-on-Chip

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DES
Dependable
Embedded Systems

Outline

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- ✓ Technology Evolution and Yield
- ✓ Reliability and Maintainability of Systems
- ✓ Application Examples
  - Circuit Design: Printed OTFT Display Drivers
  - System Design: Networks-on-Chip
- ✓ Dependable Embedded Systems: Concepts for Research
- ✓ Closing Remarks & Strategic Conclusions

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Power Consumption

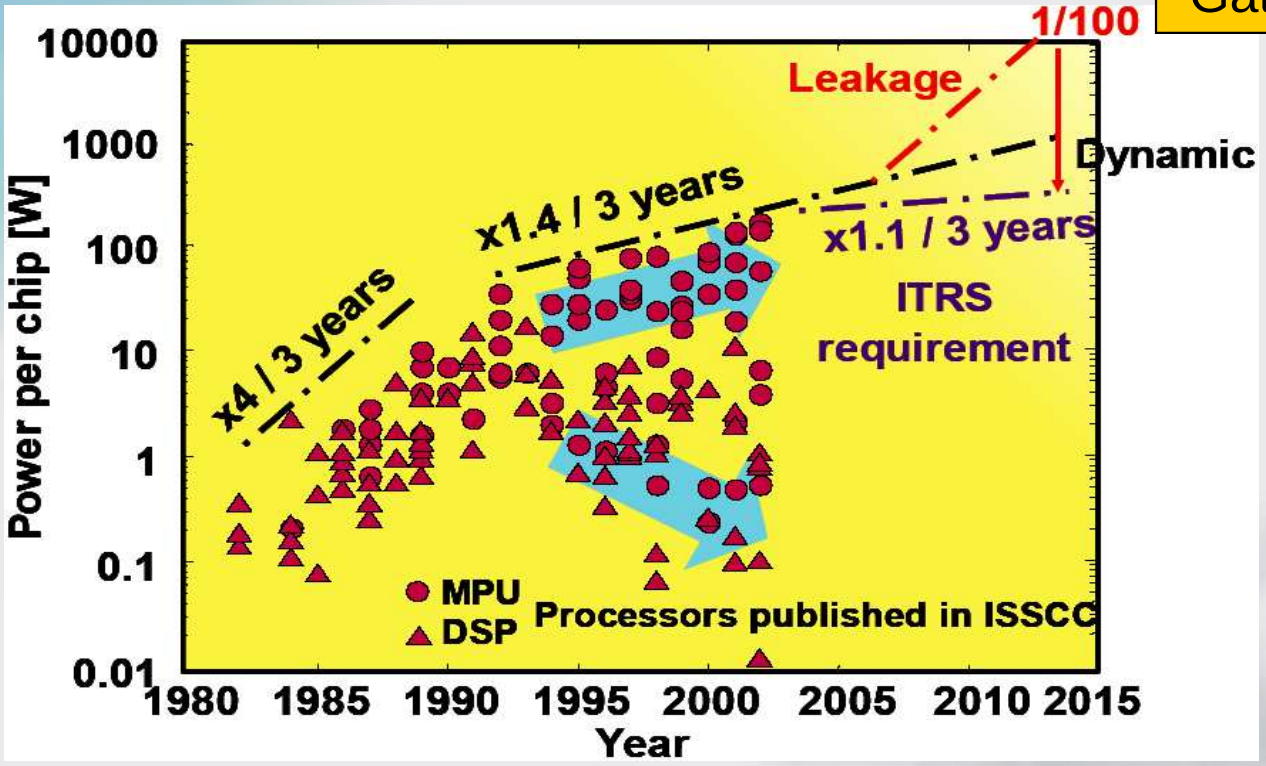
- ✓ Traditionally: **the driving force behind technology changes!**
- ✓ Currently: **rapidly-growing power densities (90 nm and beyond)**
  - Causes: **exponential growth** of

Bipolar → NMOS → CMOS

Subthreshold

Gate Leakage

currents



[Source/Copyright: Sakurai 2004 ISSCC]

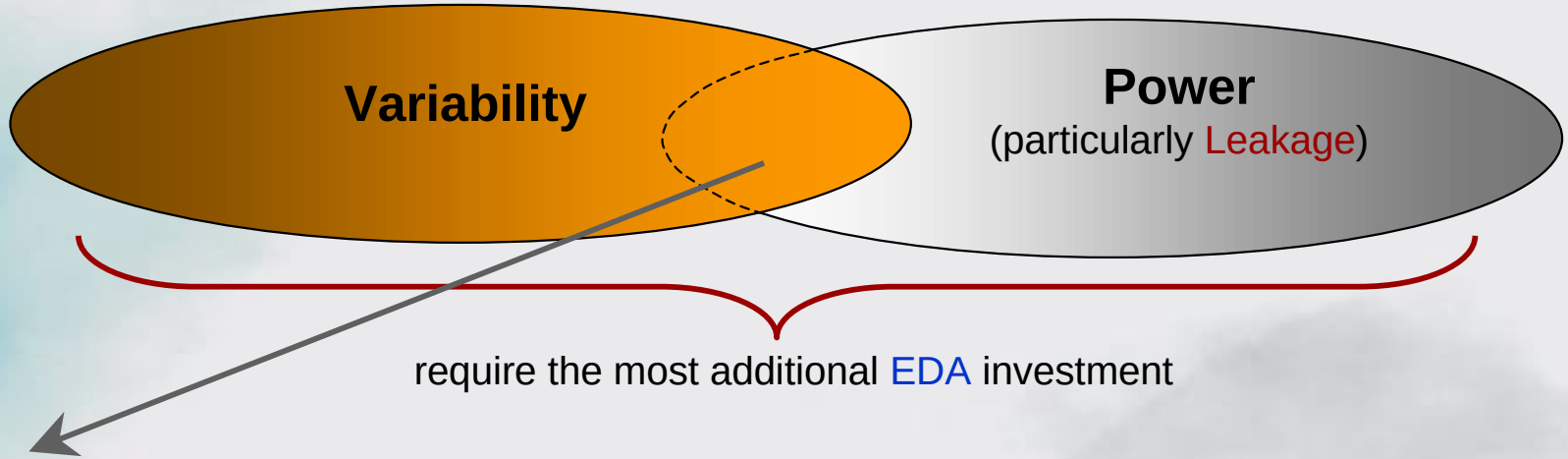
Research for a mature low-power

Technology Alternatives to Silicon-CMOS:

- ✓ Single electron transistors
- ✓ Spin transistors
- ✓ Carbon nanotube FETs
- ✓ Ferromagnetic logic devices

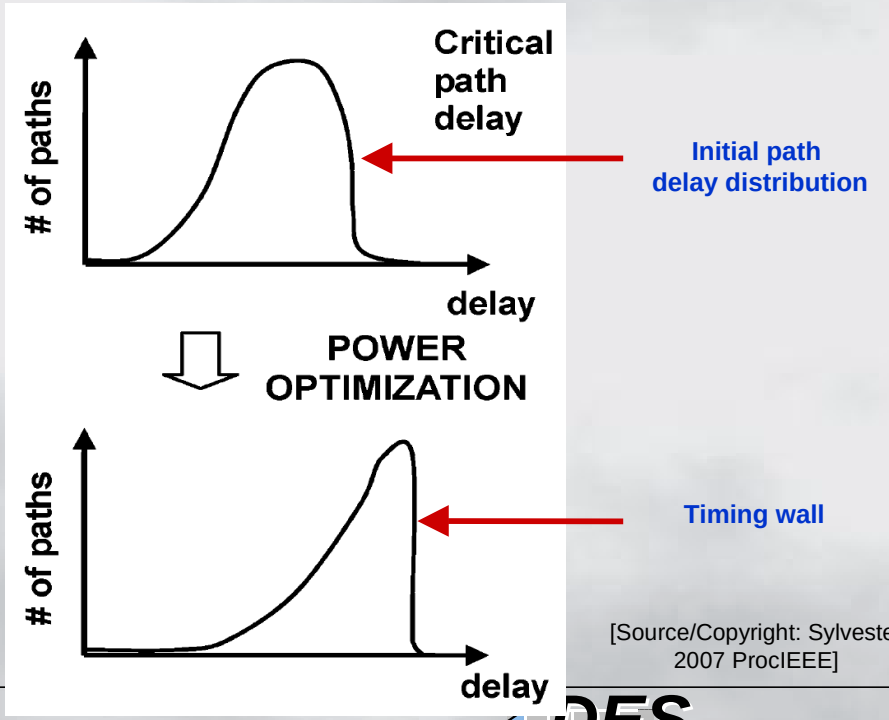
⇒ 10 ... 20 years

Power vs. Variability



- ✓ Inherent Tradeoff: Critical Delay
  - Initially: many noncritical delay paths
  - Power optimization: distribution pushed towards the initial critical path delay
- ✓ (Near-)Critical Paths:
  - affect the yield due to

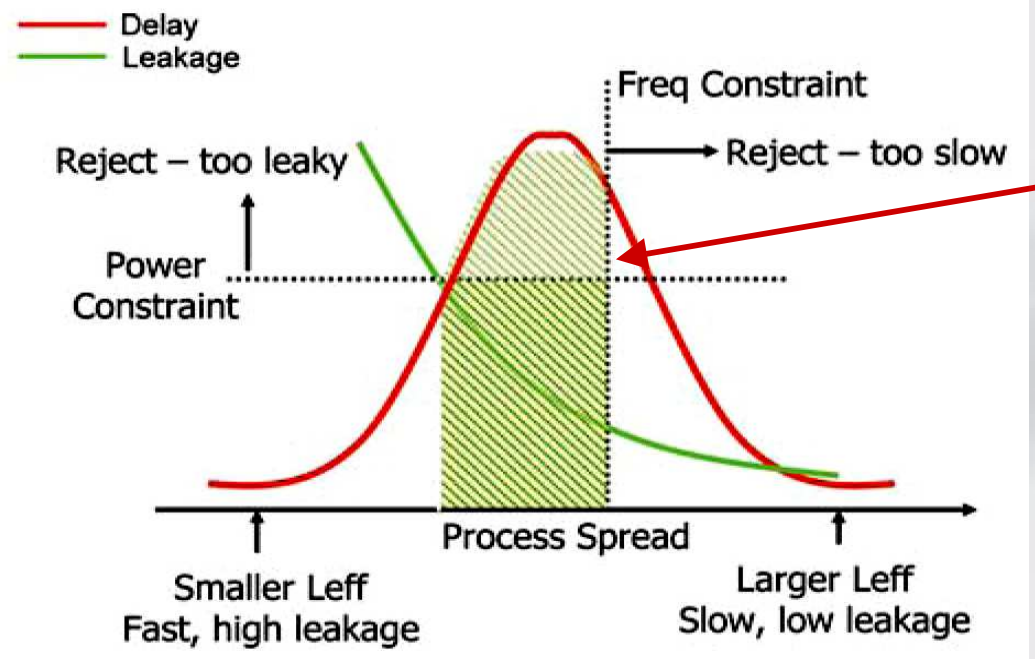
Process Variability



[Source/Copyright: Sylvester 2007 ProcIEEE]

Quantifying the Tradeoff

- ✓ Parametric Yield given Timing and Power Constraints:



Two-sided yield constraint

Leff: effective channel length

[Source/Copyright: Sylvester 2007 ProcIEEE]

Delay **Leakage**

inversely correlated: opposite sensitivities to Leff

- ✓ Major Concern: **yield loss due to power constraints violation**
  - Leff variations affect:

Dynamic Power	sublinearly
Leakage Power	exponentially !

Challenge: Power Density

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Hot Plate

- Power: 1500W
- ∅: 180mm
- Area: 25400mm^2
- **Power Density: 0,059W/mm^2**

Infineon/Qimonda: Advanced Memory Buffer, 2006

Source/Copyright:Infineon

- Power: 6W
- Die Area: 30,5mm^2
- **Power Density: 0,196W/mm^2**

Power Density/Heat has a strong Impact on Reliability!

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DES Dependable Embedded Systems

Basic Definitions

- ✓ Reliability:

  ... is the ability of a system or a component to perform its required functions under stated conditions for a specified period of time (IEEE)

- ✓ Robustness

  ... is the quality of being able to withstand stresses, pressures, or changes in procedure or circumstance. A system, organism or design may be said to be "robust" if it is capable of coping well with variations (sometimes unpredictable variations) in its operating environment with minimal damage, alteration or loss of functionality. (Wikipedia)

Reliability: Devices, Components, Systems

Device + Device + Device + ... = Component

$$R_{C_j} \leq \prod_{i=1}^{N} R_{Di}$$

Component + Component + Component + ... = System

$$R_{S_k} \leq \prod_{j=1}^{M} R_{C\,j}$$

Example: $0.99^{10} = 90.4\%$ $0.99^{100} = 36.6\%$

- ✓ **Technology Issue**:
  solve reliability problems in new technologies; adequate technology modeling
- ✓ **Device Issues:**
  appropriate device models; device and circuit simulation; robust ciruit design
- ✓ **Circuit Design Issue**:
  cope with limited device reliability >> device tolerant design techniques

Reliability: Devices, Components, Systems

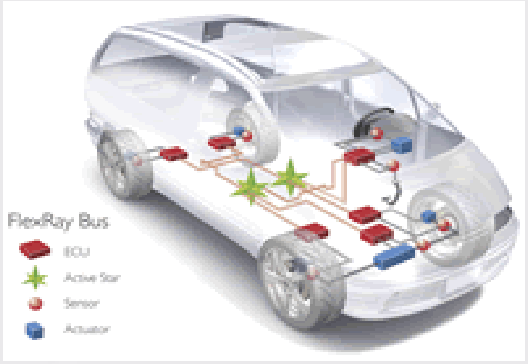
- ✓ System Design Issue:

  robust specifications, architectural fault tolerance, in-system diagnostics,

  flexible adaptive systems with masking capability for lower level deviations/defects

- ✓ Application Design Issue:

  select adaquate manufacturing technologies, design techniques and system architectures



Source/Copyright: NXP / Spoerle

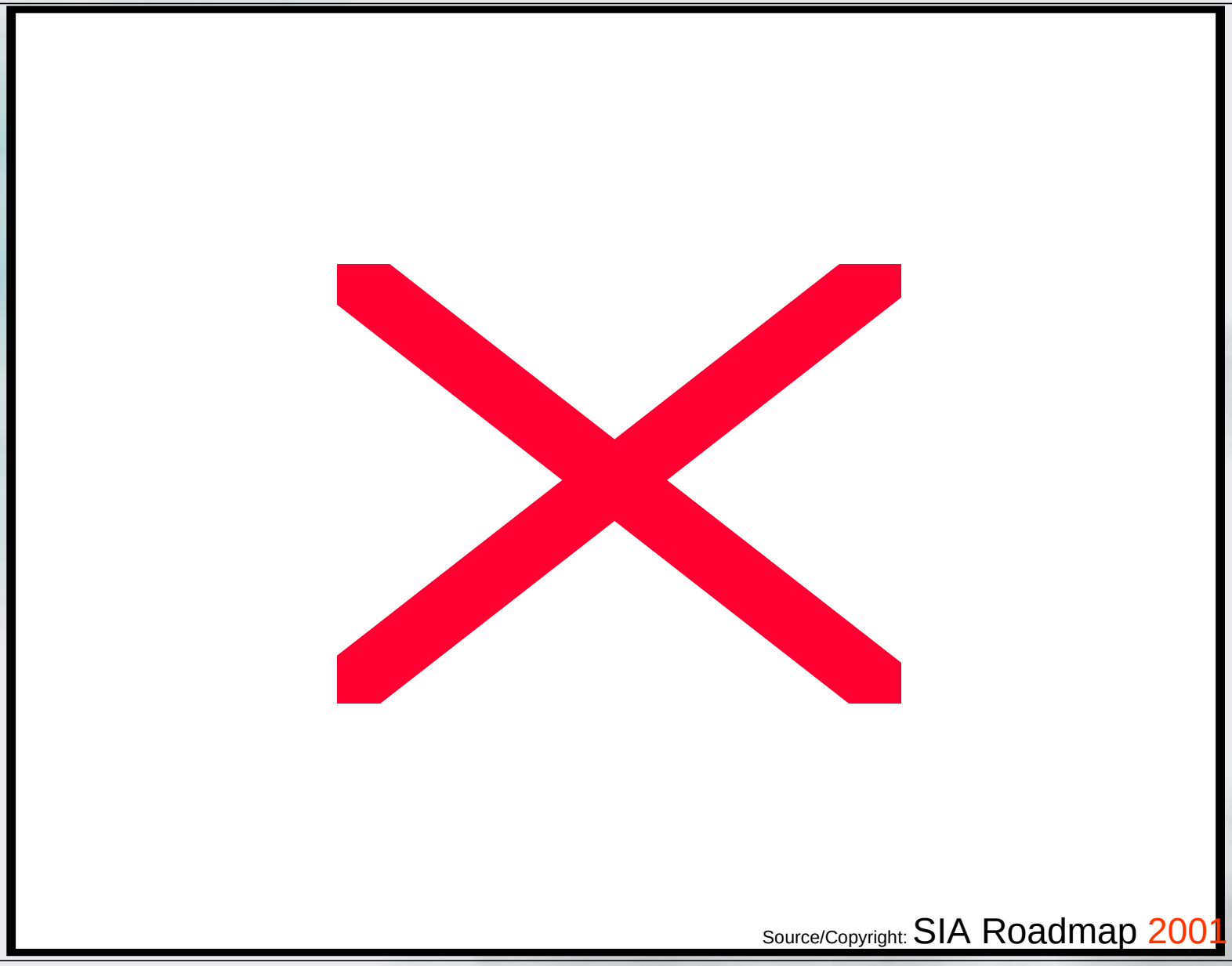
Source/Copyright: sees-project.net

- ✓ Test / Quality Control Issue:

  test, if guaranteed system functionality is available

Physics / Technology → Models → Test

Productivity Gap: Technology vs. CAD



Source/Copyright: SIA Roadmap 2001

Productivity vs. Reliability

- ✓ Productivity increase by
  - use of CAD
  - re-use of components

Source/Copyright: porsche.com

needs an extensive effort in specification management and specification propagation over several levels of a system design

in order to achieve **functional reliability!**

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Application Requirements vs. Technology

Requirements: Active Matrix Driver for OLED Signage Display

- Pixel Area = Available Size for driver circuit
- Digital Signage: low dynamic requirements (W of transistors can be rather small - just the required current has to be driven)

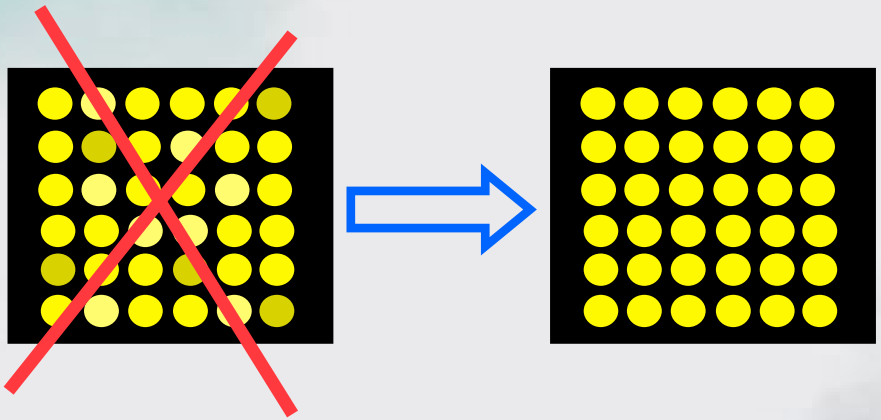
Source/Copyright:www.vizworld.com/tag/display/

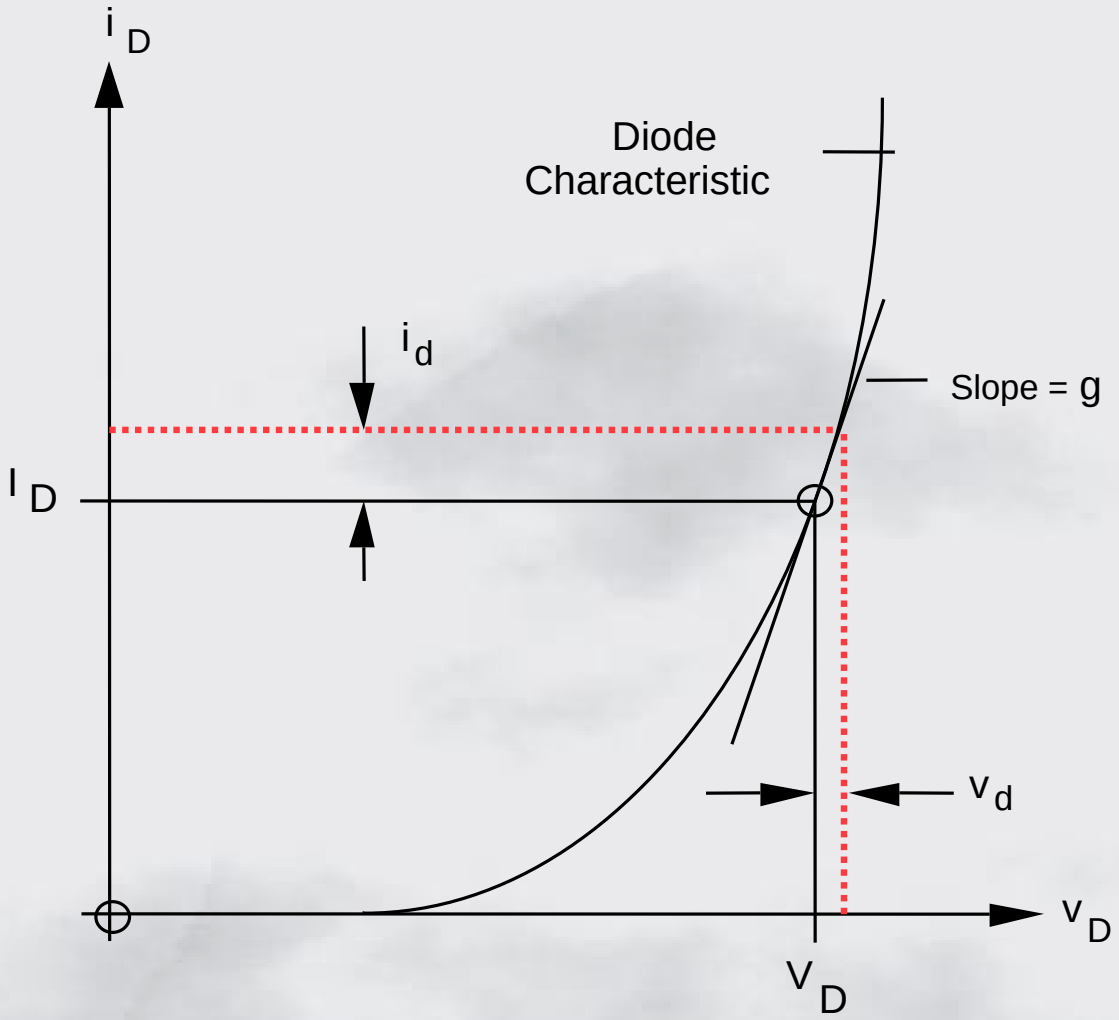
Application Requirements vs. Technology

Additional Requirements: Active Matrix Driver for OLED Signage Display

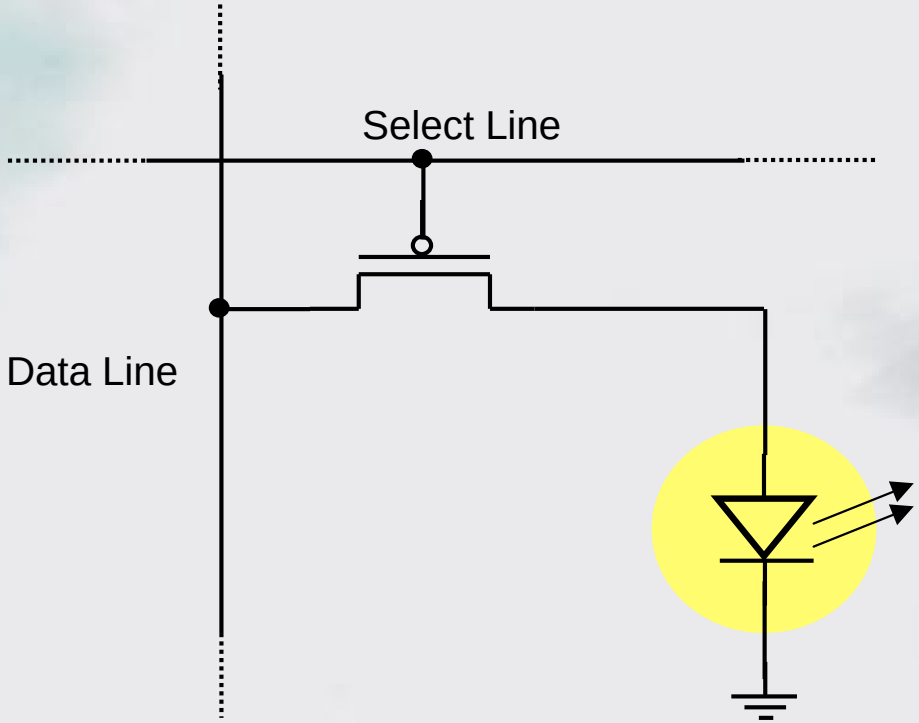
Uniform image area shouldn‘t be „cloudy“

- OLED current control instead of voltage control
- requirement of compensation of the driver transistors V_T and contact resistance variations caused by the process





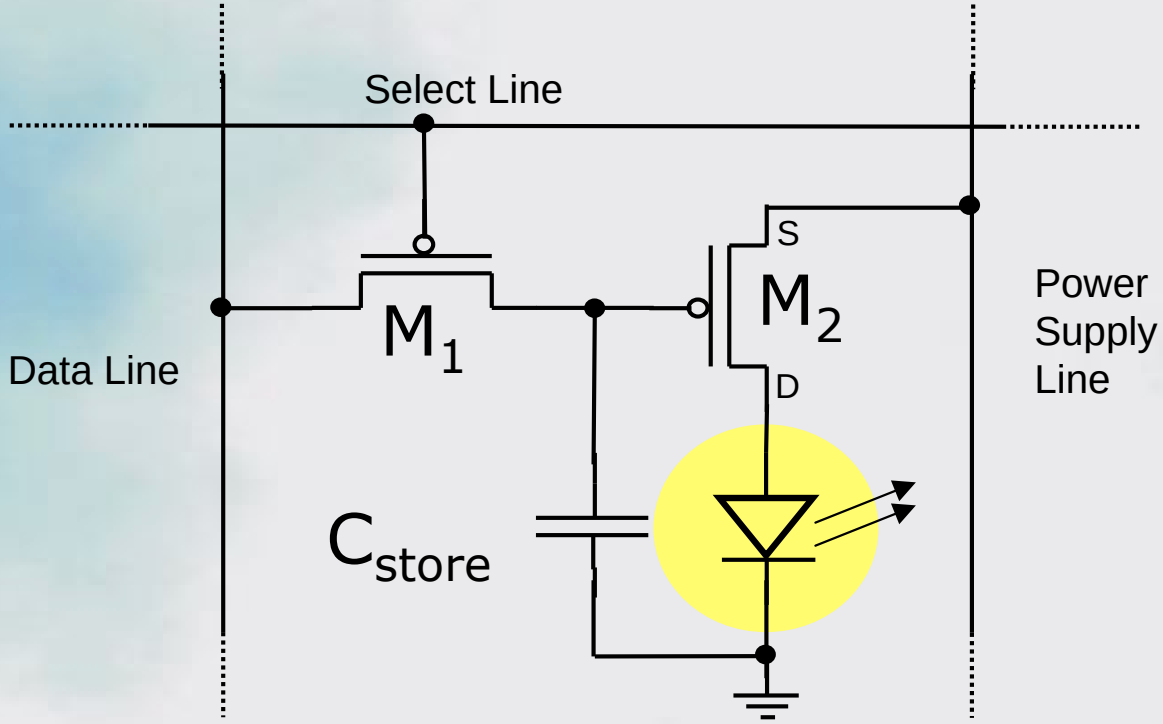
One Transistor Solution



Disadvantages:

- Doesn‘t support row/column scanning
- OLED is voltage controlled
- Not robust against parameter variations

Two Transistor Solution



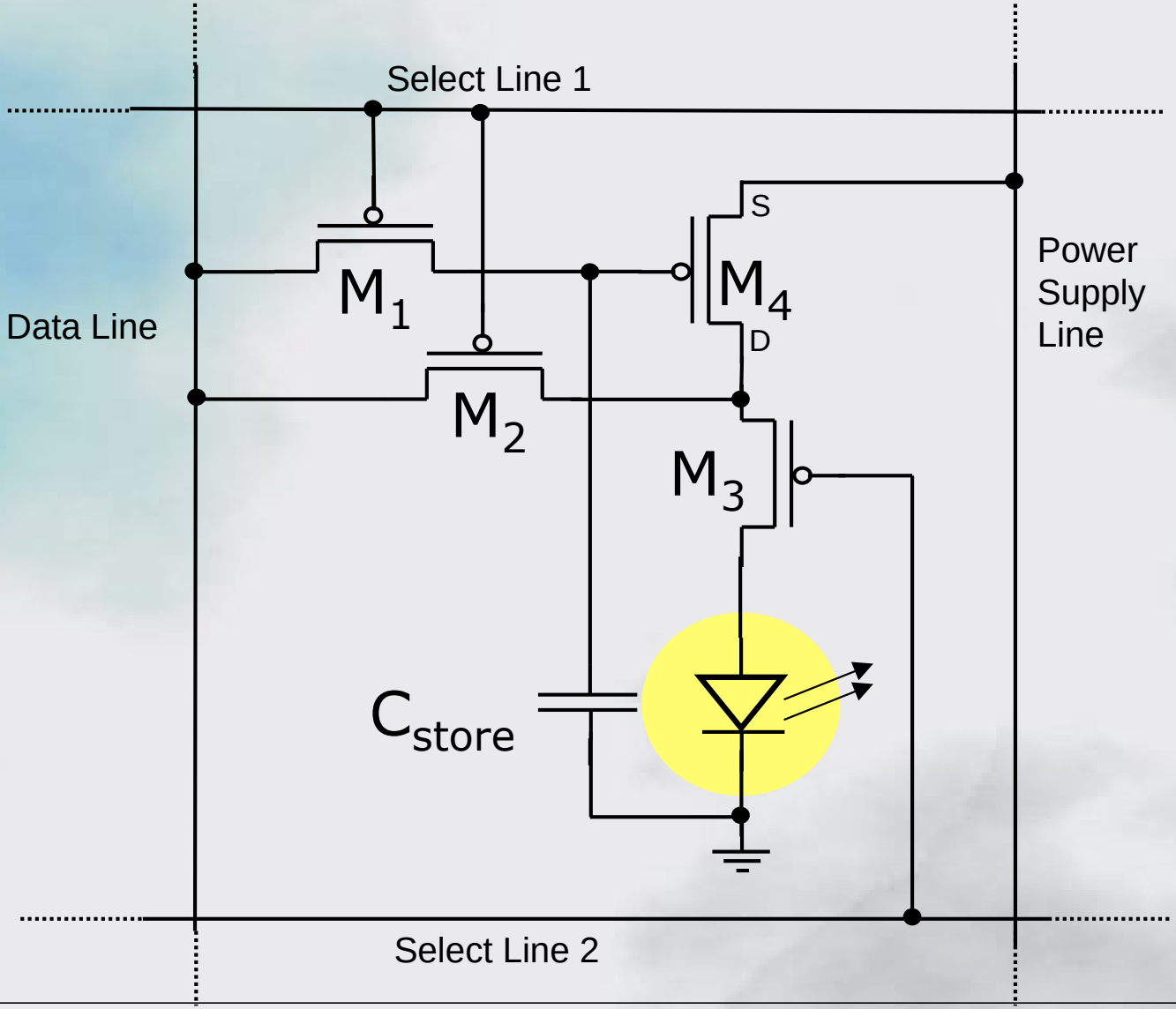
Disadvantages:

- Not robust against parameter variations

Dimensioning Flow:

- Required Brightness defines necessary OLED current I_{OLED}
- related OLED voltage V_{OLED} can be extracted from OLED characteristics
- $V_{DS,M2} = V_{OLED} - V_{DD}$
- Guess M_2 operation mode
- Dimension W of M2
- Compute required V_{GS} of M_2 from current equation.
- Check if operation mode guess was correct

Four Transistor Solution



Operation:

- Set Select Line 1 to Low and Select Line 2 to High
- M_4 goes into Saturation Region
- Impress exact current over data line (V_{GS} of M_4 relaxes to value according to current equation in saturation region)
- Set Select Line 1 to High and Select Line 2 to Low again

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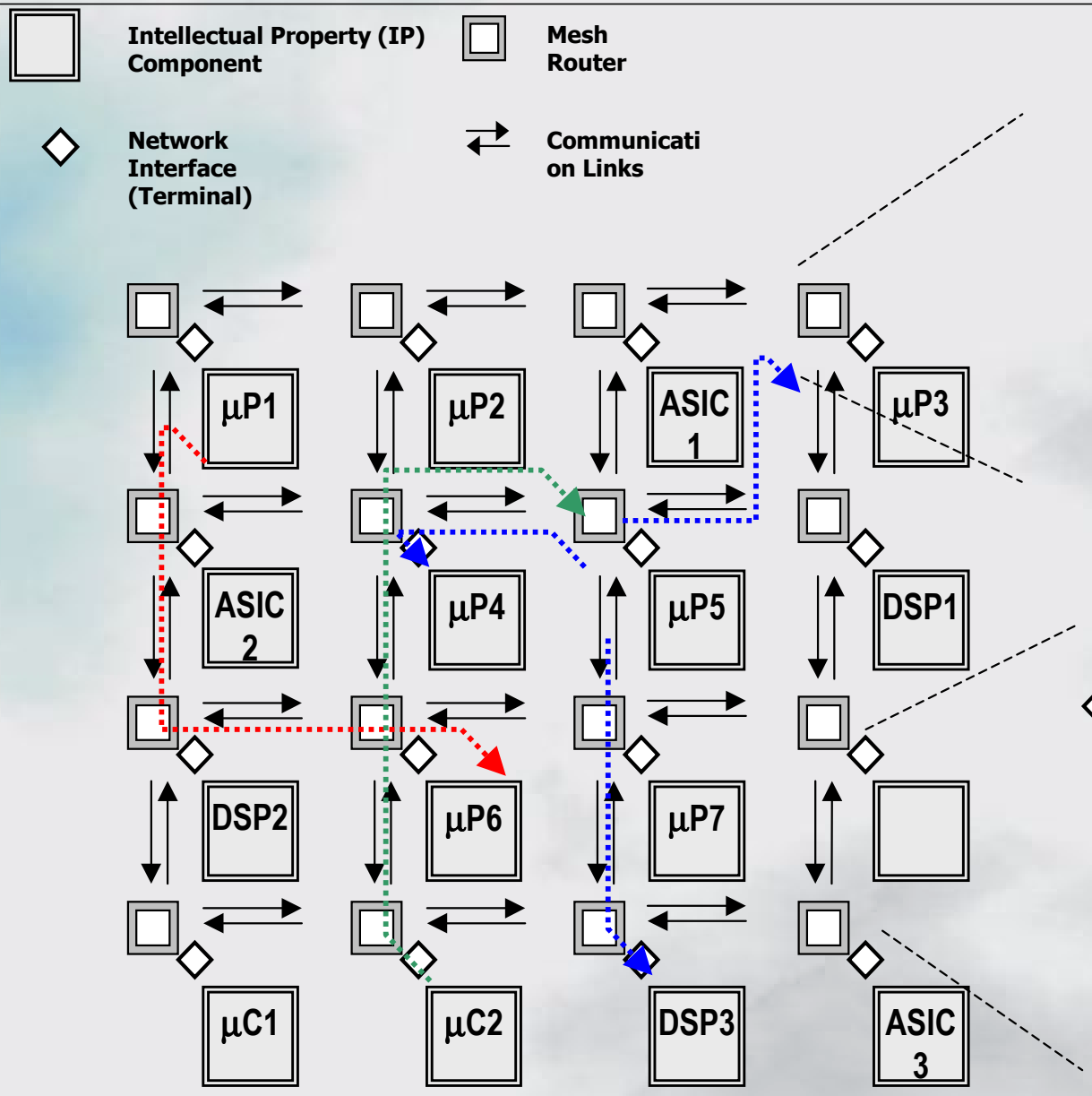
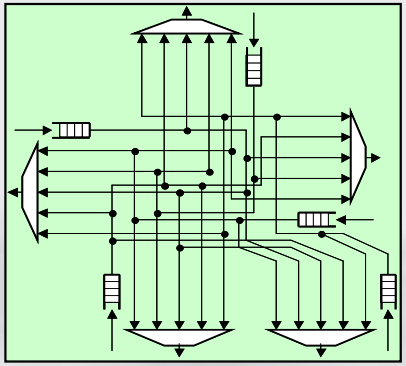
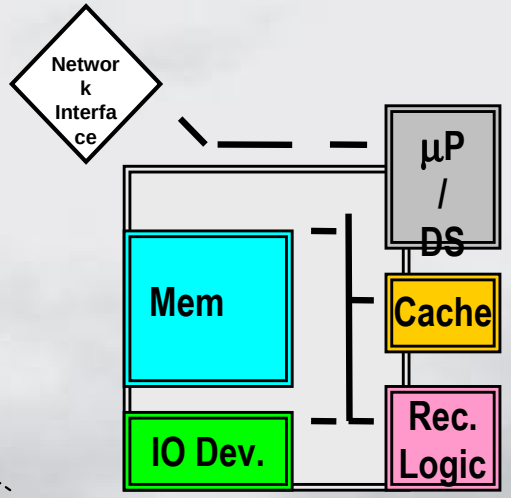
Network-on-Chip with 4x4 Mesh Topology





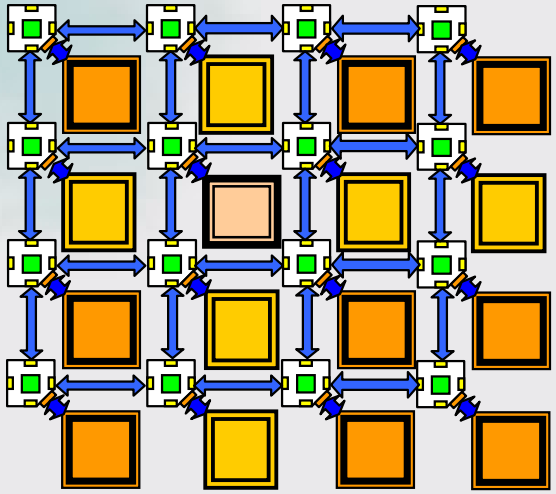
Mesh Switch Router

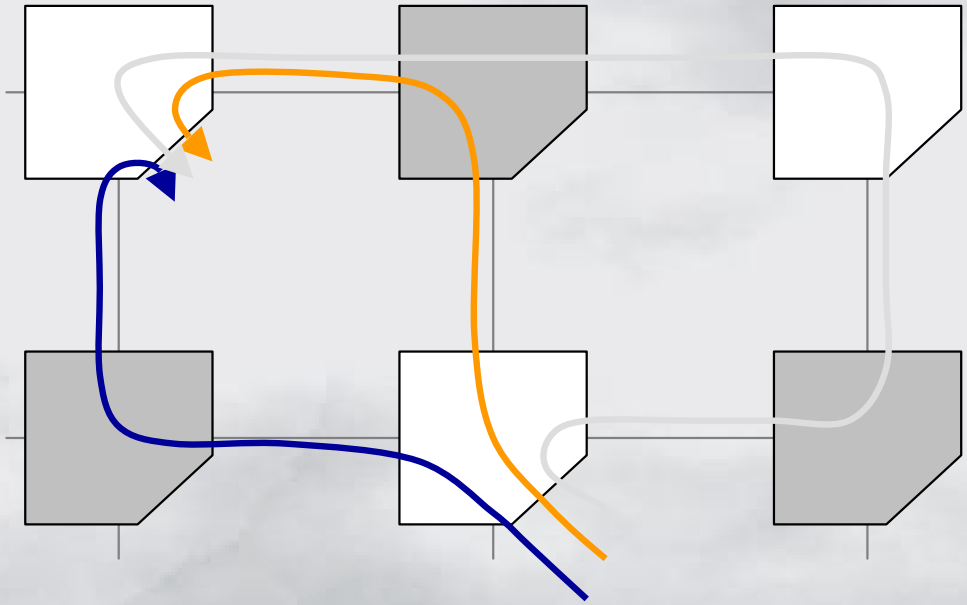


NoC Routing Design Objective: Adaptivity

Adaptivity for increased reliability / fault tolerance and power flexibility:

- Multiple pathes can be used for routing from a source node to a target node
- Adaptive circumvention of defective network links
- Network adaptation in case of partial power shut-down
- Maximized performance by adaptive traffic equalisation on network links





Routing: Deadlock Avoidance - Virtual Channels

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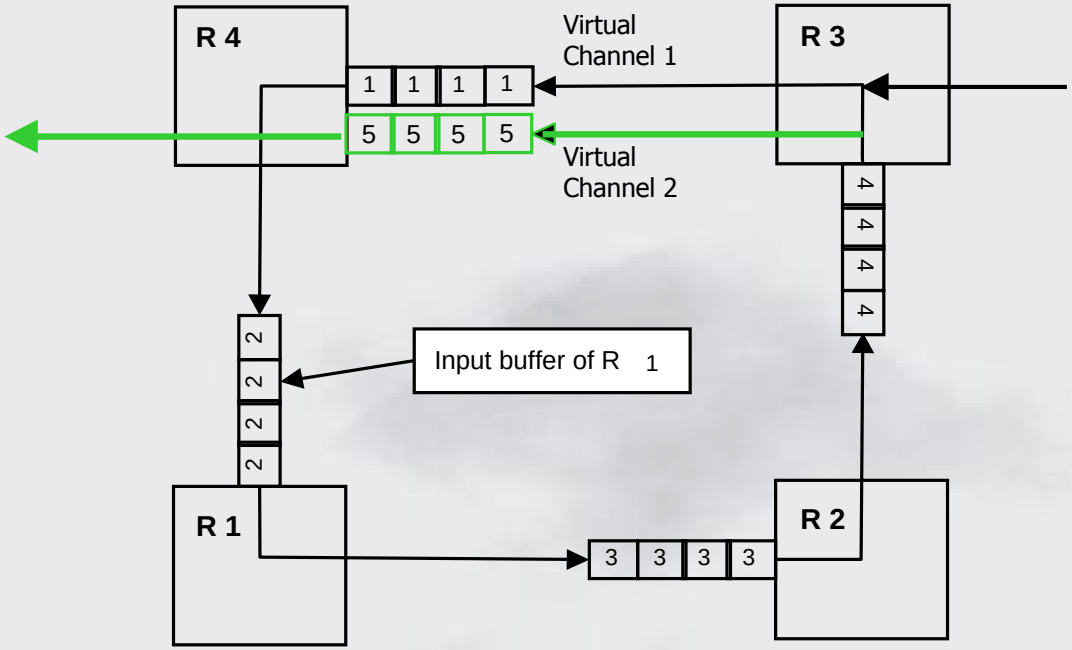
Deadlock Avoidance:

- Introduction of Virtual Channels (e.g. Duato,); Disadvantage: complex switch fabric (large router area)
- Goal: avoid cycles by principle! (Problem: this goal is competing with adaptivity!)

Livelock Avoidance:

- Mimimum Routing would avoid livelocks



Routing algorithms, that do tolerate a large variety of irregularities and which don't apply the concept of virtual channels have to fulfil the condition of absence of cyclic dependencies and provide maximum adaptivity!

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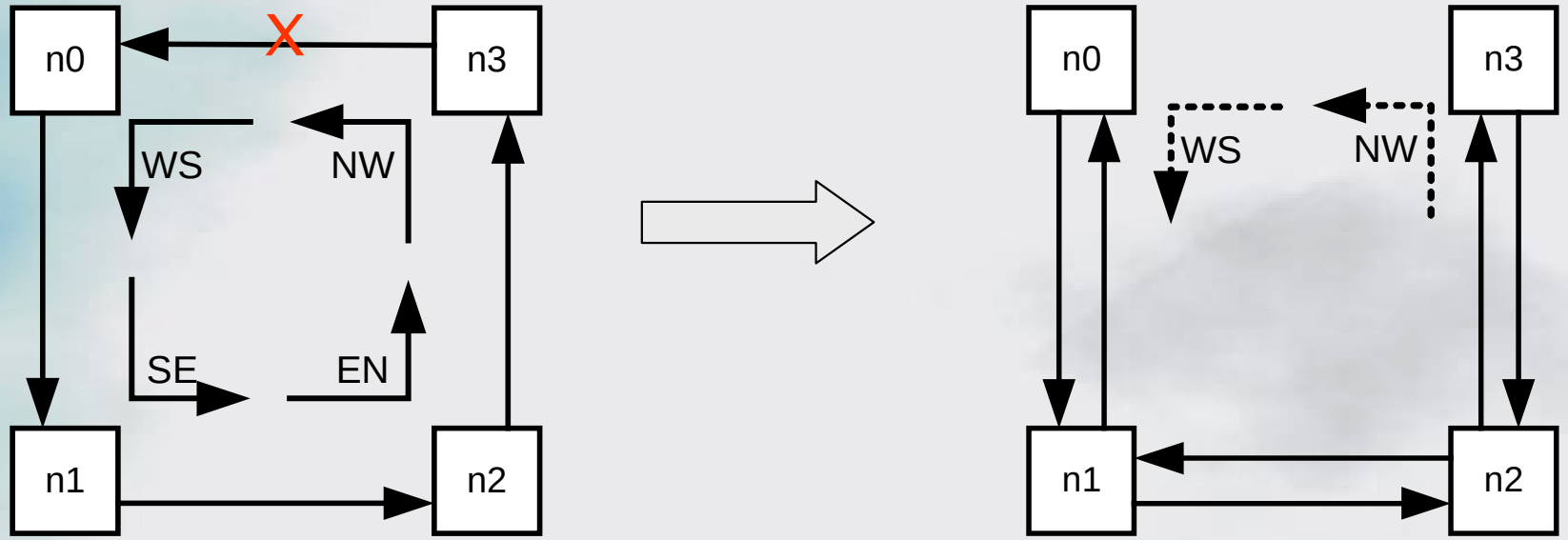
Deadlock Avoidance: Turn Theory

Prohibition of "turns" destroys cycles to prevent deadlocks



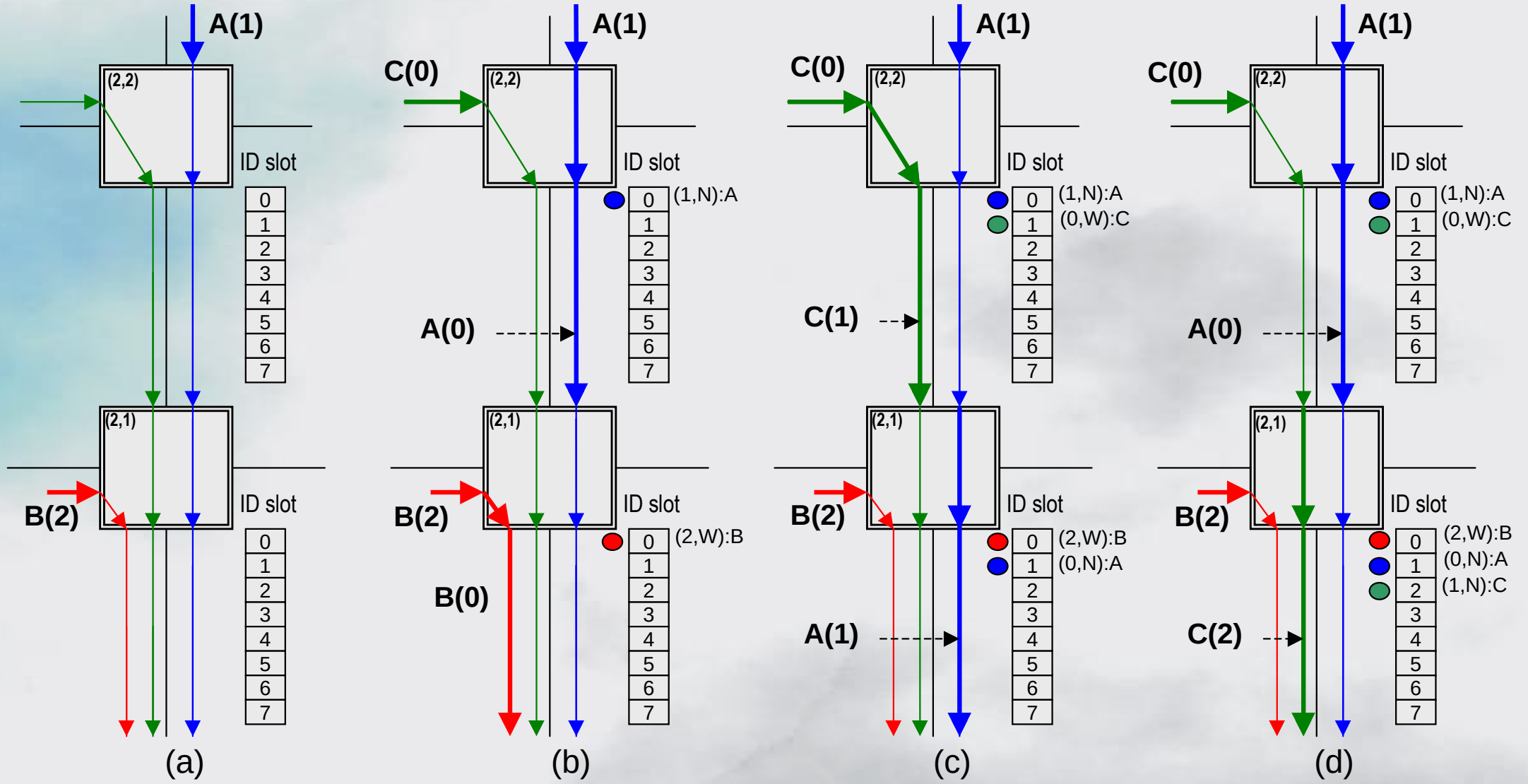
State-of-the Art:

Glass, C.J. and L.M. Ni: The Turn Model for Adaptive Routing,
Proceedings of the 19th Annual International Symposium on Computer Architecture, 1992

Chiu, Ge-Ming: The Odd-Even Turn Model for Adaptive Routing,
IEEE Transactions on Parallel and Distributed Systems, 2000

Wu, Jie: A Fault-Tolerant and Deadlock-Free Routing Protocol in 2D-Meshes Based on Odd-Even Turn Model,
IEEE Transactions on Computers, 2003

Link Setup by XHiNoC

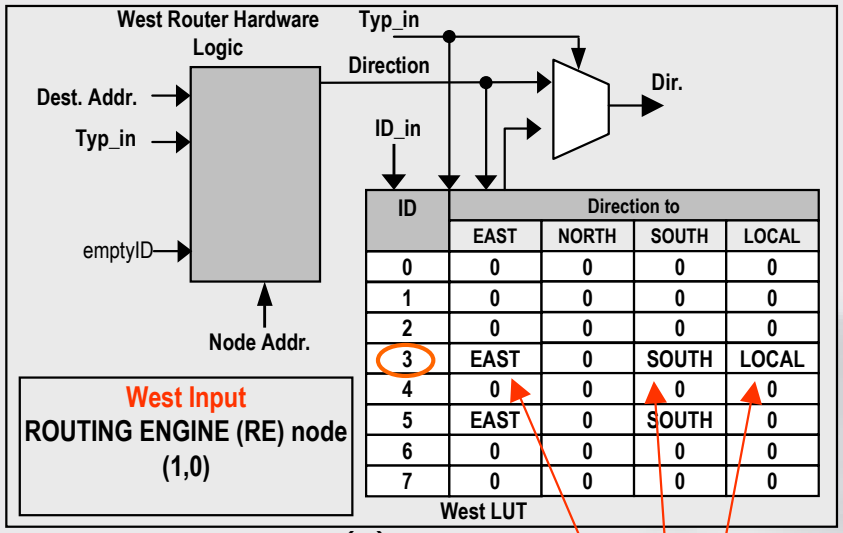


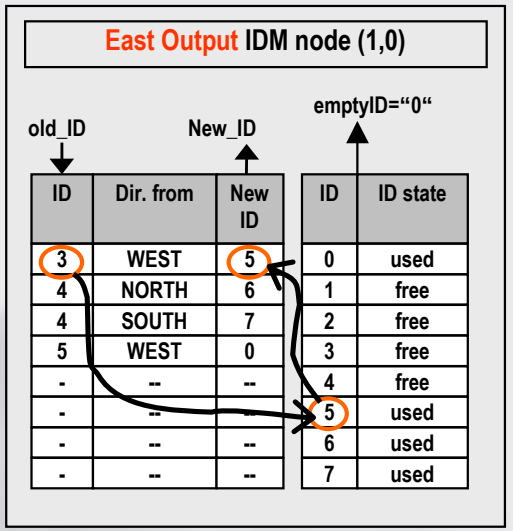
XHiNoC: Packet Interleaving and Multicast Capability

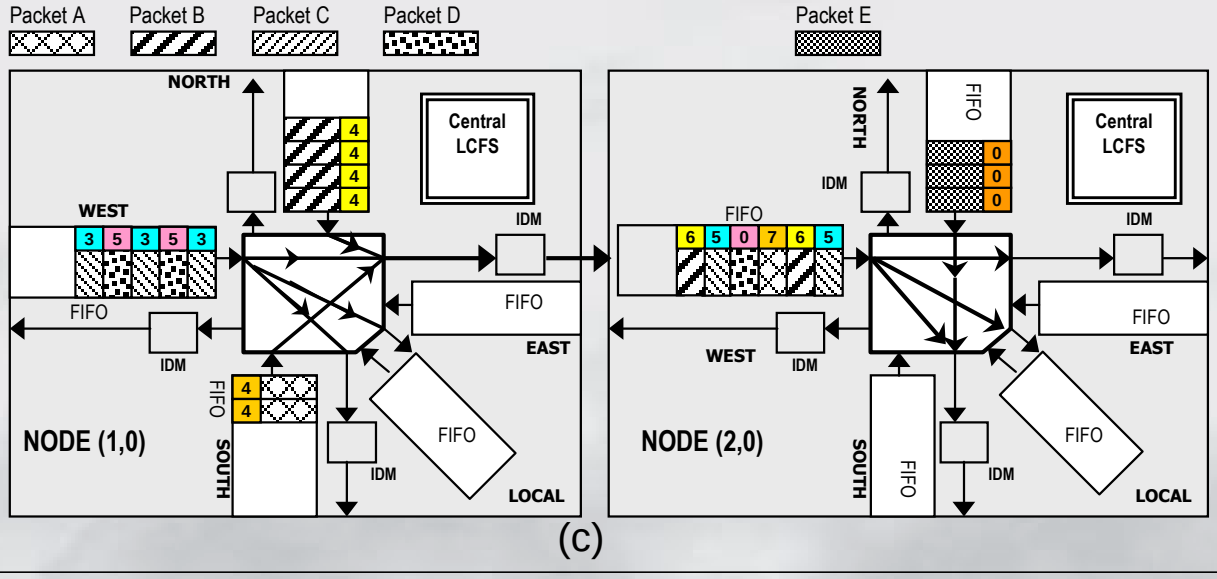
The Routing Engine (RE) is combination of a flexible router hardware logic and a reconfigurable router look-up-table (LUT).

IDM unit maps ID slot allocation and classifies flits based on their ID-tag.

The emptyID signal is set to '1' if there is no free ID-tag and is sent to router hardware logic.







Scalability: Network Size, Power (partial shutdown)

Robustness against Soft Errors

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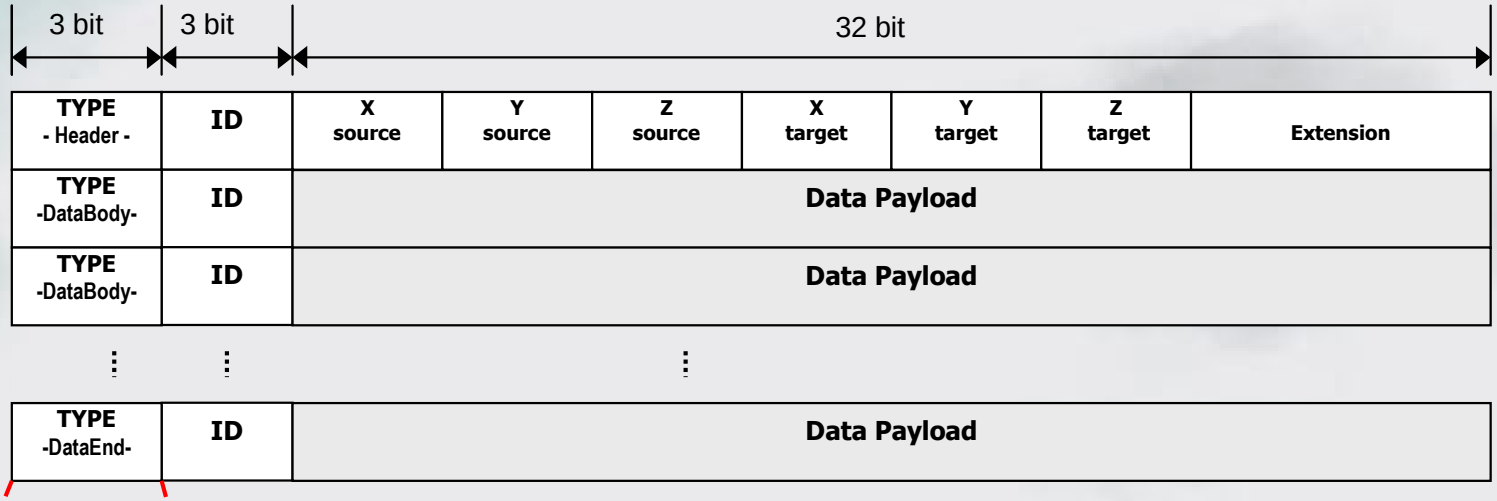
These bits have to be secured against soft errors on physical level, otherwise misrouting will occur by the ID mapping of the network

For data / payload bits it may be sufficient to secure them by CRC checks on application level



Type of Flit	bin/dec code
Not FLit	000 (0)
Packet Header	001 (1)
Message/Data Body	010 (2)
End of Message	011 (3)

NoC-specific provisions have to be considered in order to target dependability

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NoC Robustness

- ✓ Defective Links: appropriate deadlock-free routing must be secured
- ✓ Hardware State must be detected and stored. Specific initialisation of NoC after BIST during power-up by Defect Management Controller
- ✓ System Reconfigurability is prerequisite for efficient Defect Management

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Dependability: Definition

- IFIP WG10.4 on Dependable Computing and Fault Tolerance:

  ... the trustworthiness of a computing system which allows reliance to be justifiably placed on the service it delivers ..."

- IEC IEV 191-02-03 (more general):

  "... dependability (is) the collective term used to describe the availability performance and its influencing factors : reliability performance, maintainability performance and maintenance support performance ..."

Design Challenges

How can we handle **Complexity**, **Power** Minimisation, technological **Variability**, computational **Throughput** and **Cost**, **guaranteeing reliability**?

- ✓ Well-defined Specification & Design Methodologies
- ✓ Scalability and Flexibility (design and configuration) Reconfigurability: Xilinx Automotive - new (Virtex) devices being highly dedicated to automotive requirements (infotainment, radar, object recognition) will occur soon

Source/Copyright:Xilinx

Functional Error Sources

Class E „externally induced errors“:

- ✓ Soft errors
- ✓ Faults caused by aging (appearing first as statistical and then as permanent faults)

Class I „internally induced errors“:

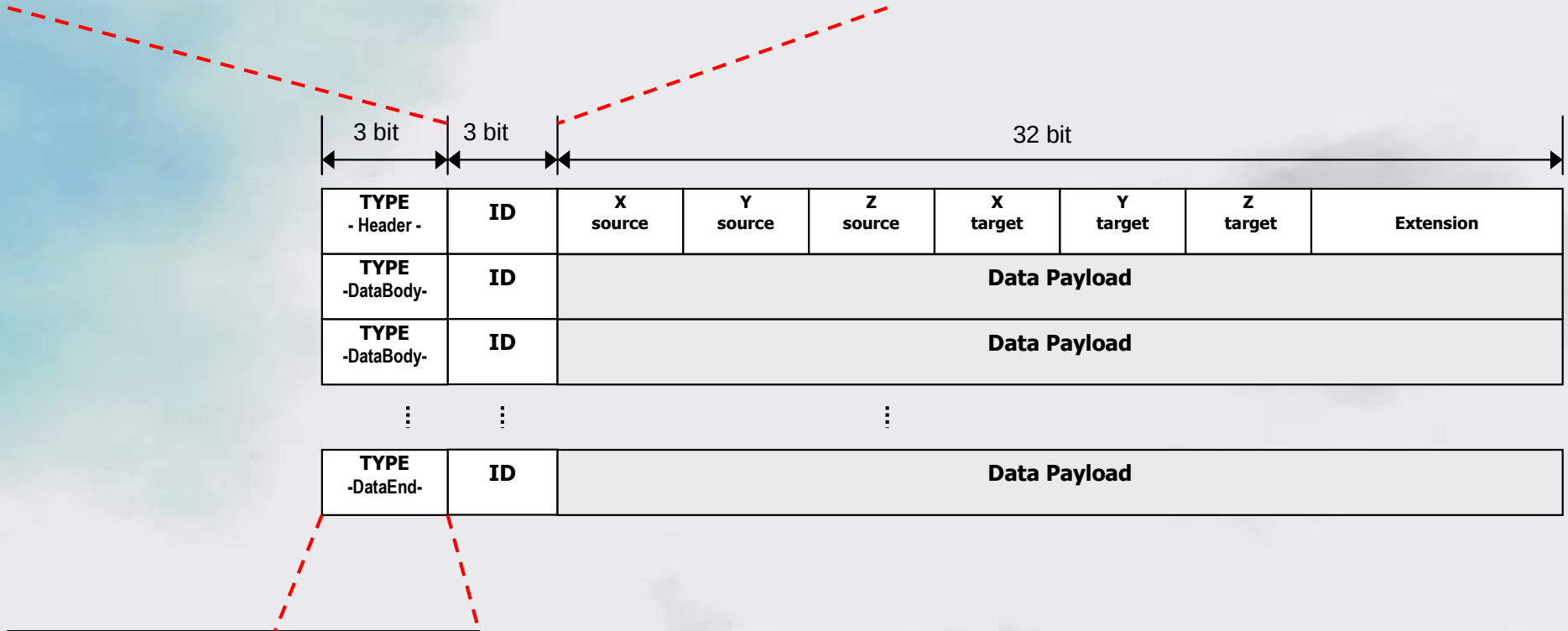
- ✓ Specification faults (lacking coverage of functional complexity)

Addressing Class E:

- ✓ Soft Error aware Design:
  - on-chip busses (physical arrangement, protocol)
  - SoC Components (redundant approaches, robust circuit structures)
  - Architecture: Adaptivity (Communication, Power)

Packet Format

Flits belonging to the same packet will have the same ID in each communication link



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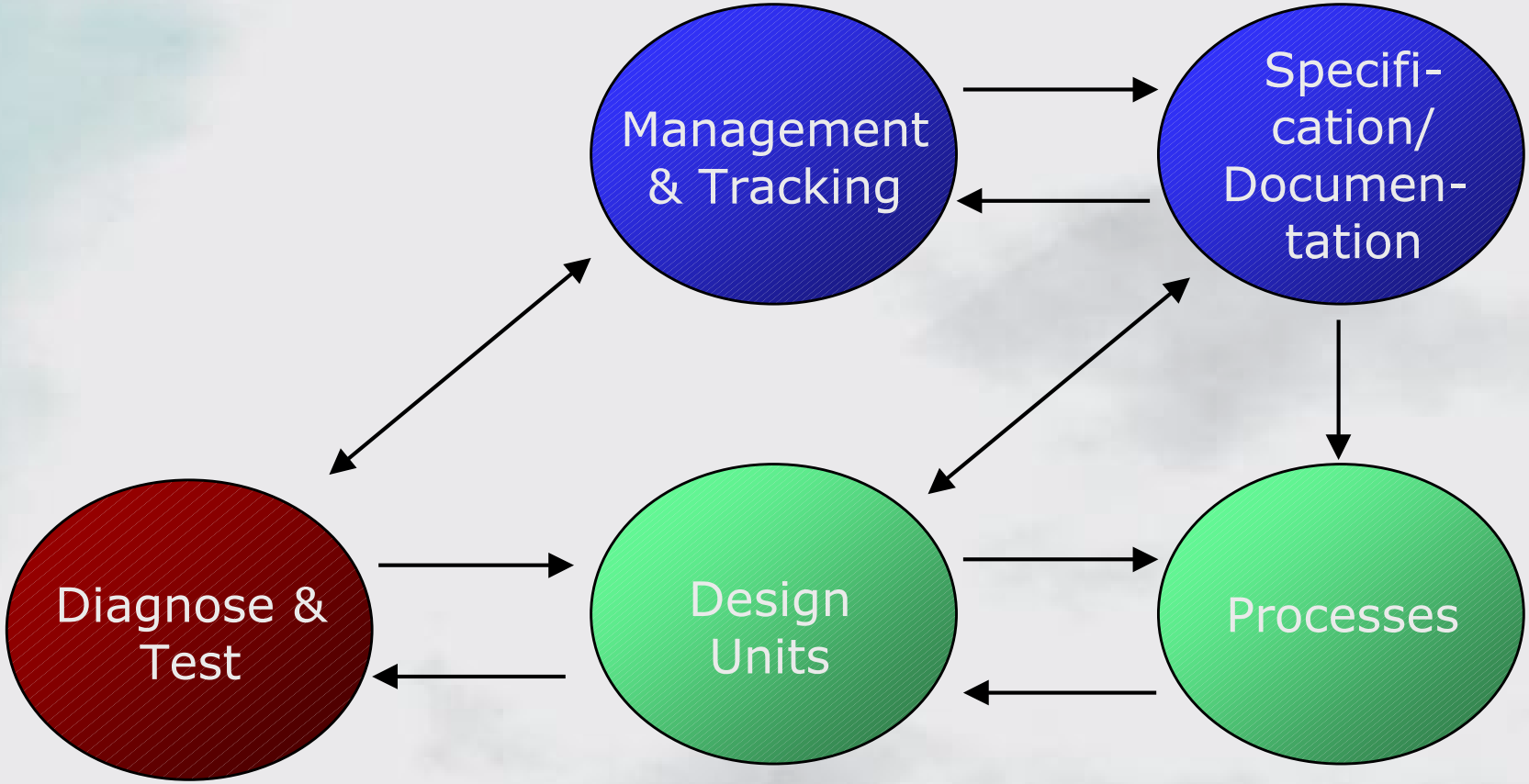
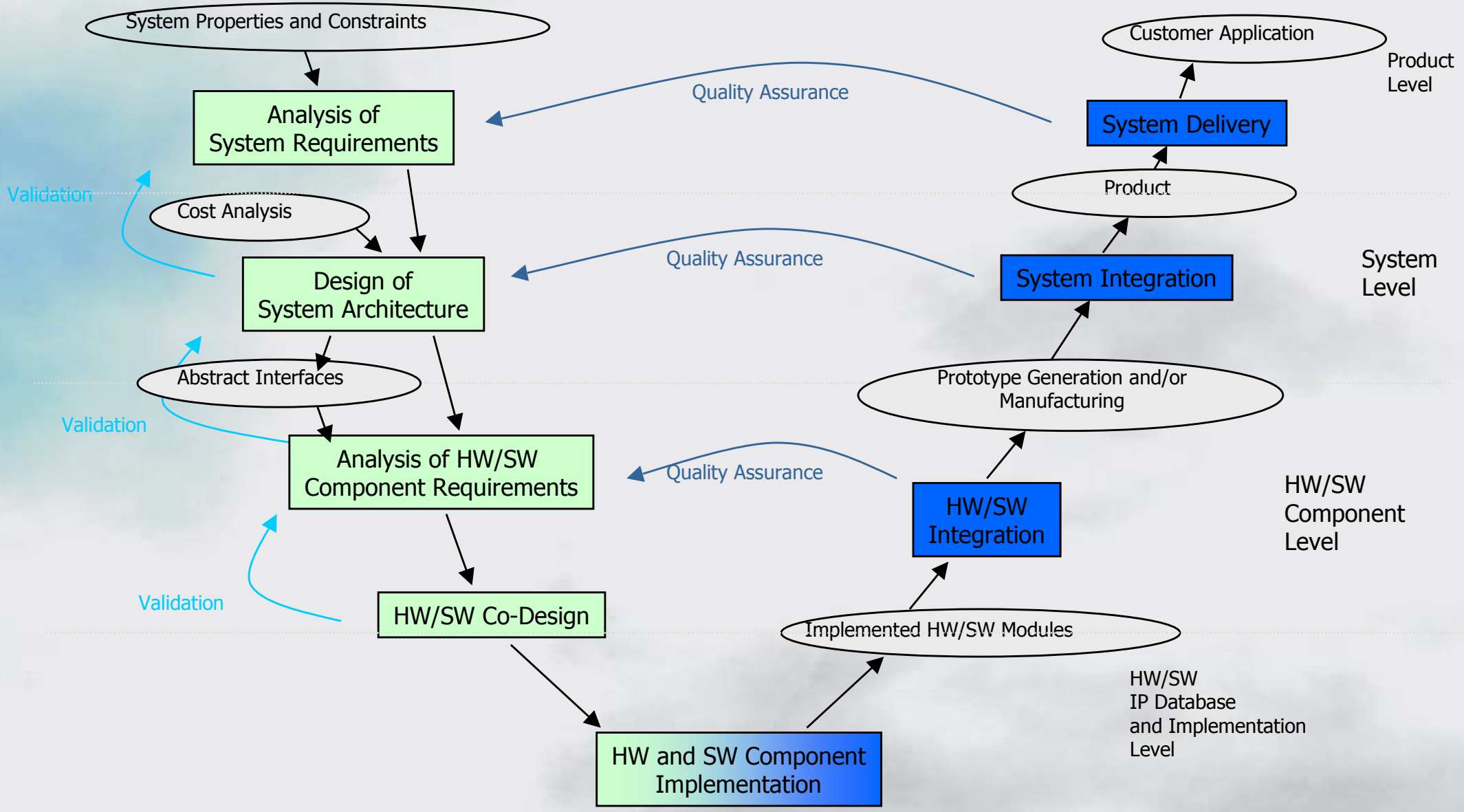
Design for Reliability



System Design: V Model



Cooperations with Research Partners

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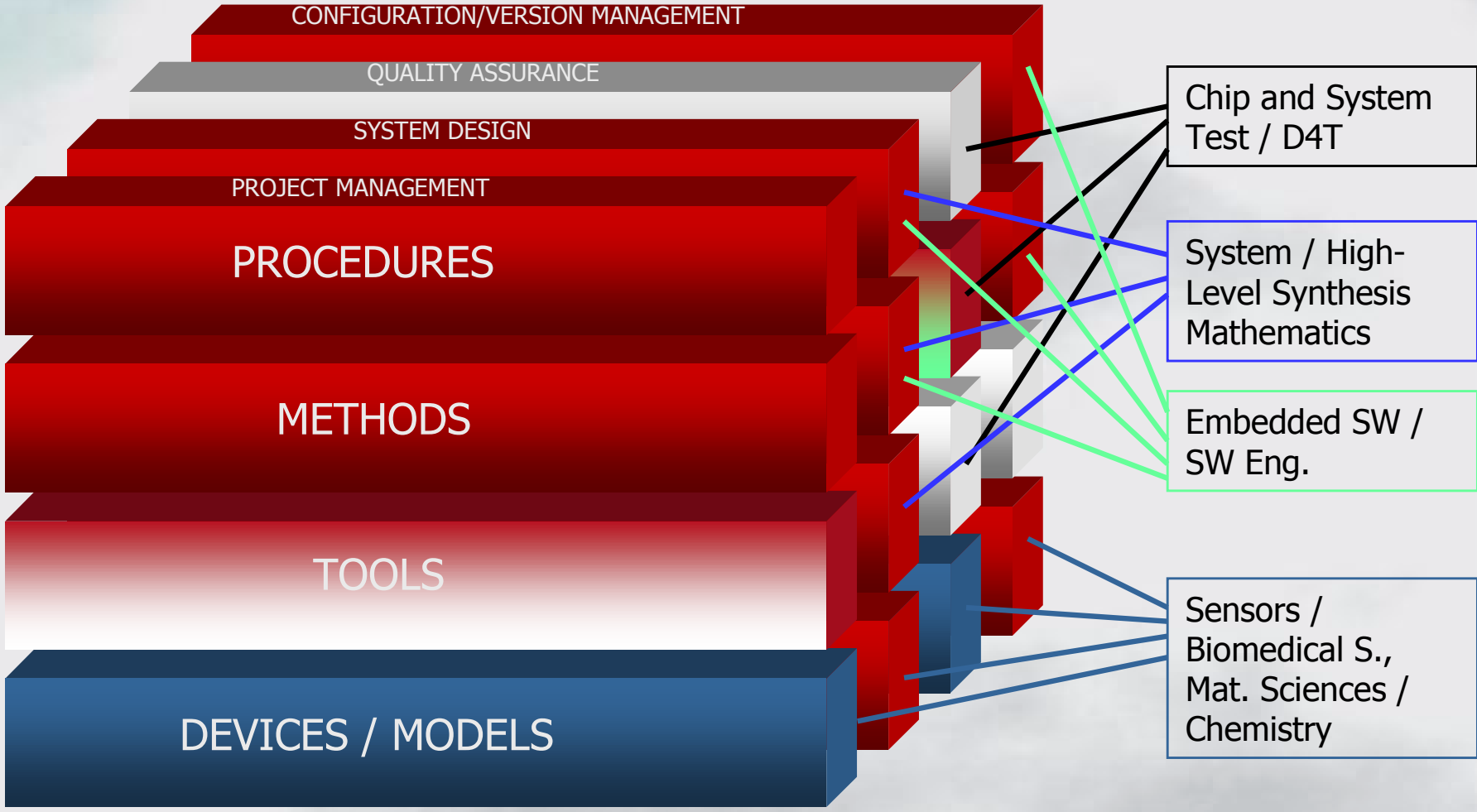

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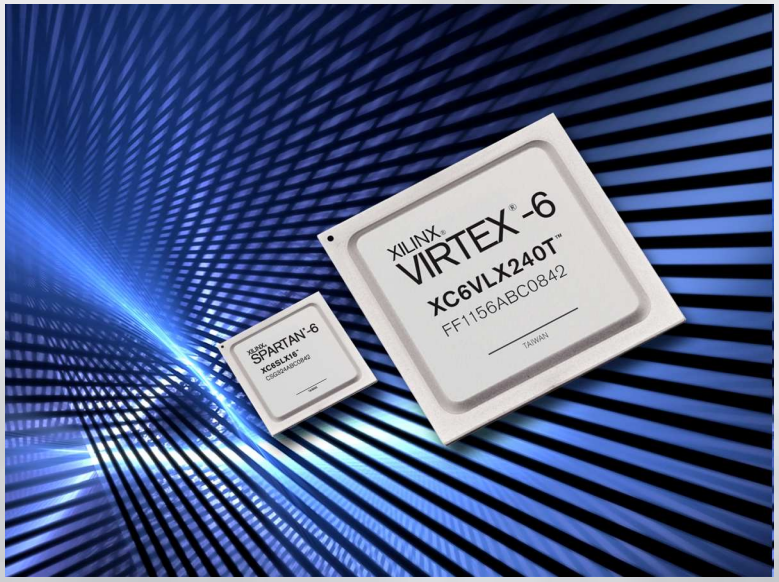
Estonian „View“

- ✓ SME Environment in the field of IT:
  - Software-driven
  - Hardware: no ASIC Industry, but reconfigurable Standard HW
  - Embedded Systems: need of Integration of HW & SW



Source/Copyright:Xilinx

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Strategic Conclusions

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Industry Orientation:

- ✓ Definition of **Research and Education Profile** based on **SME requirements** in the **environment of the university**
- ✓ Exploration of new technological possibilities can only be achieved by new **interdisciplinary approaches**

Research:

- ✓ Addressing Technology Properties and Soft Errors
- ✓ Extensive Use of Debug Systems on Chip and Board Level
- ✓ Seamless Network Integration

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Education: Computer Engineering

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Education:

- ✓ High-Tech job profile – be at the cutting edge of technology
- ✓ Integrated View: Hardware & Software
- ✓ Internationalisation of Master and Ph.D. Education

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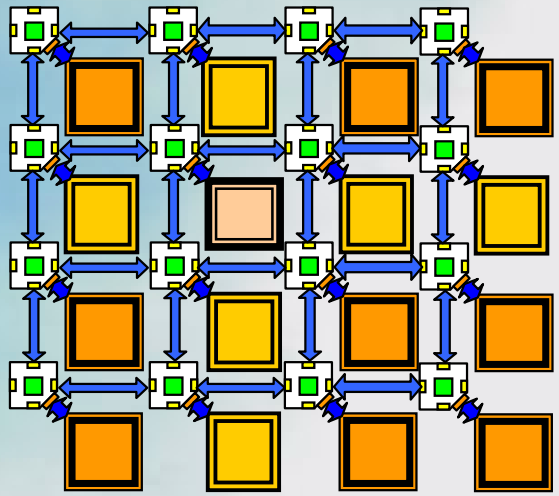

Thank you for your attention!

It‘s Time 4 your Questions now ...