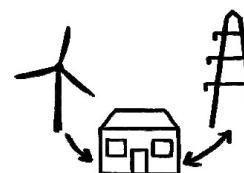
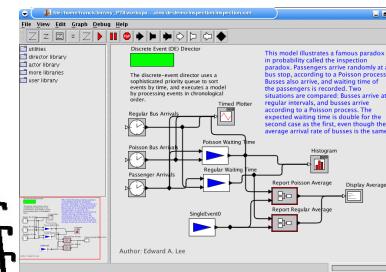
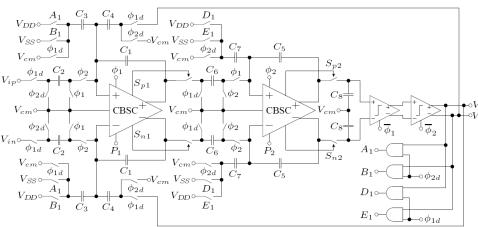
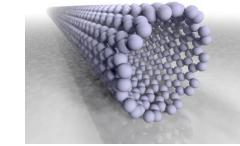
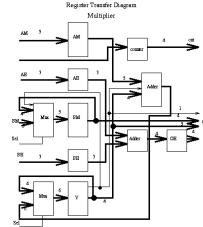
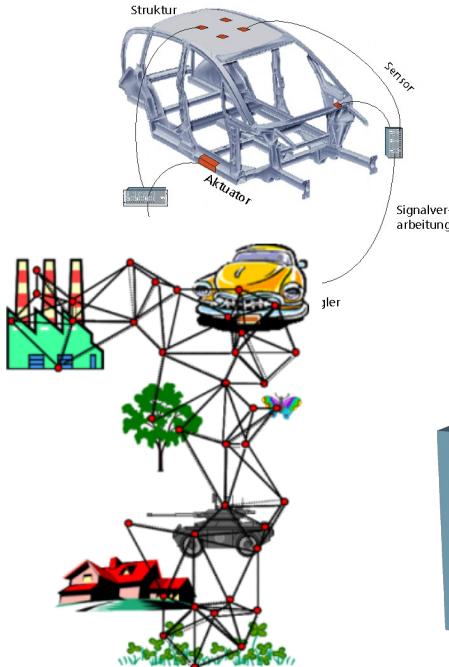


Strategic Research Directions in Electronics



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From System Design to Adaptronics and Smart Grids



Outline



- Status of the electronics industry
- Research overview @ MES
- System Design
- Strategic research directions
 - Smart Grids
 - Healthcare
 - Adaptronics
- Making the world “smart”, reliable and energy-efficient Wireless sensor networks

Quo Vadis, Electronics ?



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Source : wikipedia.de

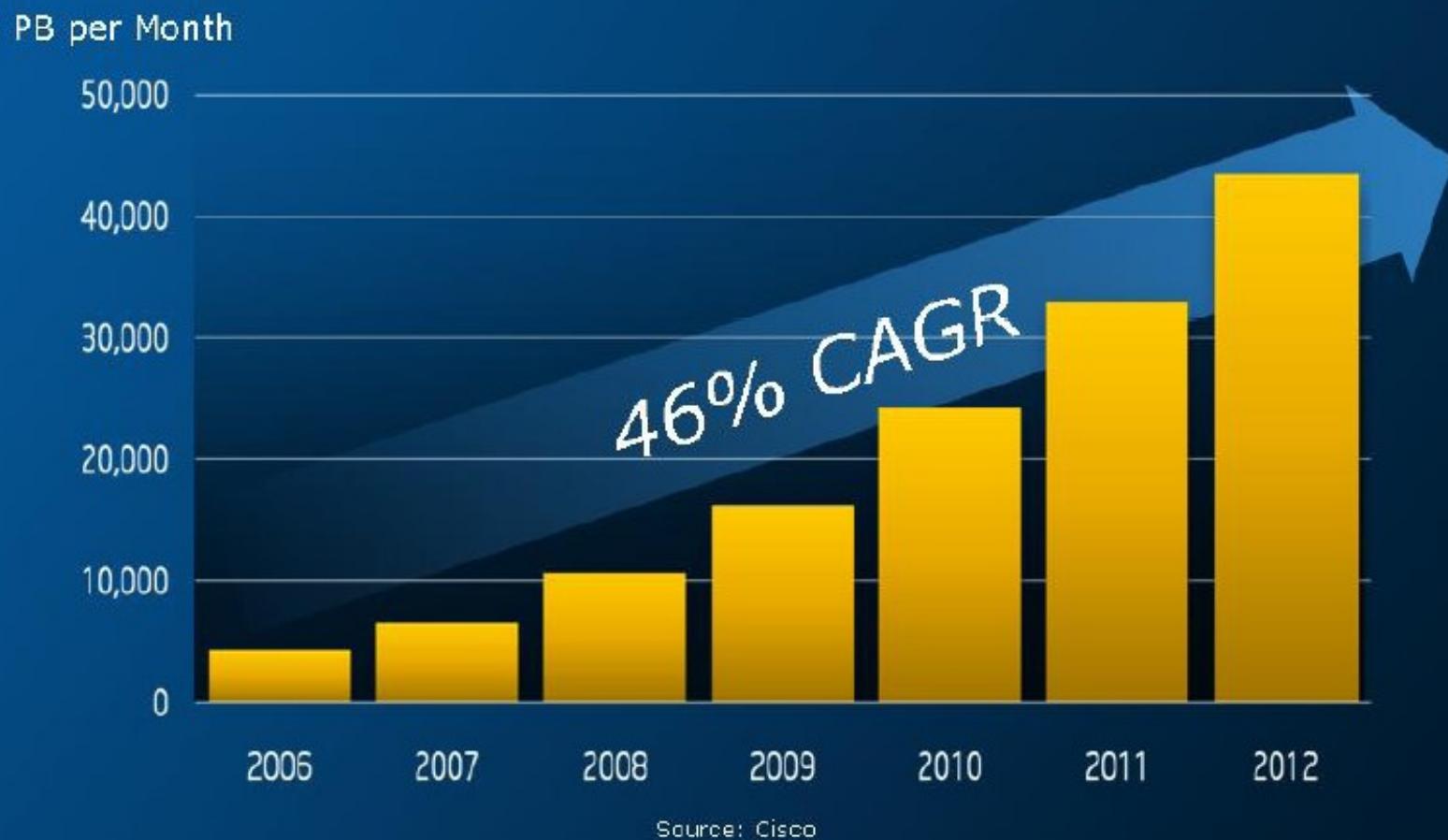
Domine, quo vadis ?
Annibale Carracci (1602)

Unde Venis, Electronics ?



- **Electronics** has been the main driving force behind the technological, scientific and economical progress in the last 50 years
- The **annual transaction volume** in **semiconductor devices** is
 - 267 Billion USD on the **world market** (Source: ZVEI forecast for 2010)
 - 8 Billion EUR in **Germany** alone (Source: ZVEI forecast for 2010)
- The **annual transaction volume** of the **electronics industry** is
 - 1378 Billion USD on the **world market** (Source: Decision forecast for 2010)
 - 160 Billion EUR in **Germany** alone (Source: ZVEI forecast for 2010)
- The electronics industry has enjoyed an **average growth rate** of **8 % per year** during the last 30 years! (Source: iSupply, Garnter 2008)

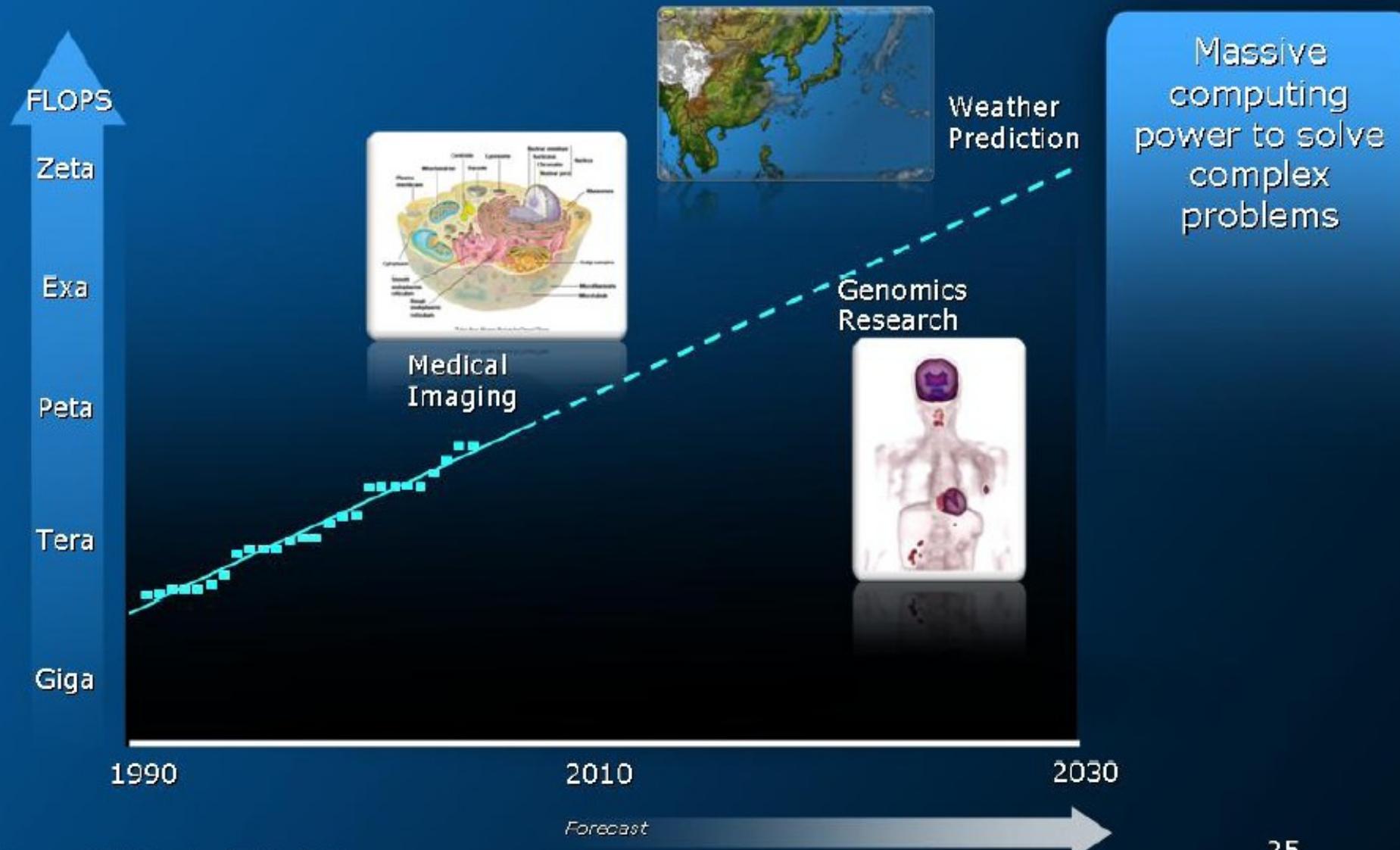
Global IP Traffic



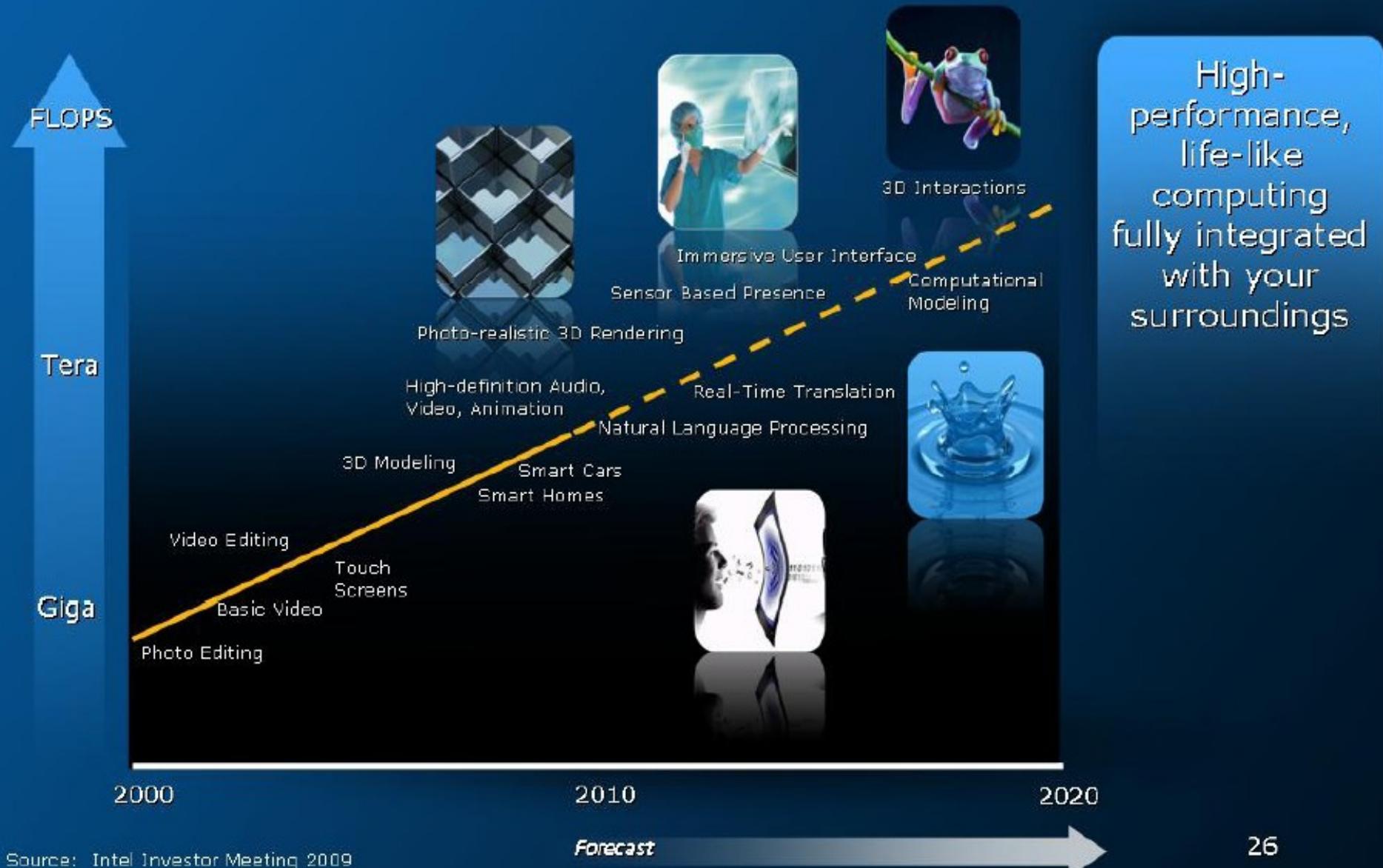
Internet Growth Continues

Source: W. M. Holt: Moore's Law Continues to Drive Innovation

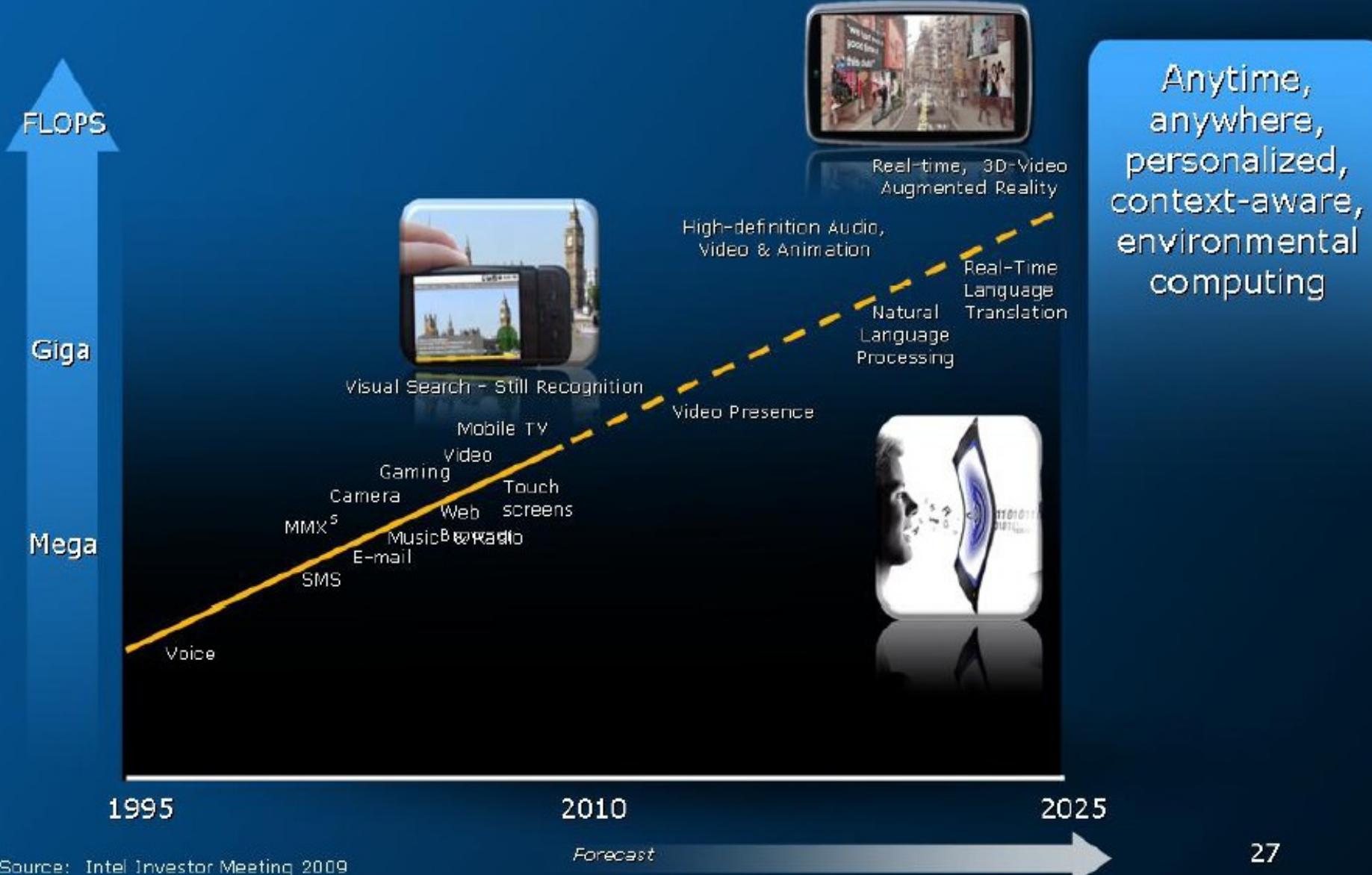
High Performance Computing Segment Needs Decades of Performance Increases



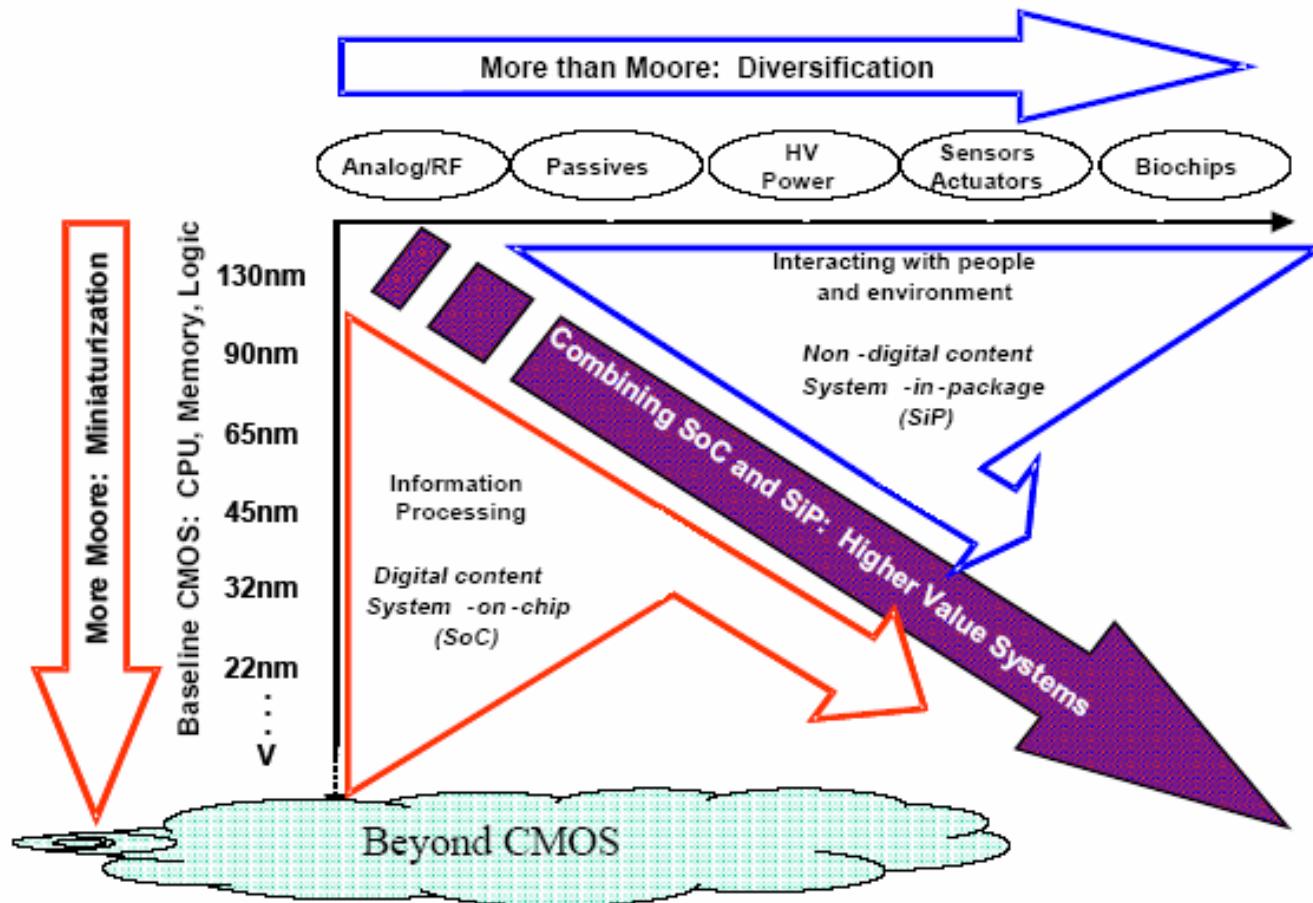
Core Computing Segment Will Need to Increase Performance to Support New Usages



Small Computing Segment Needs More and More Performance At Low Power



A Roadmap

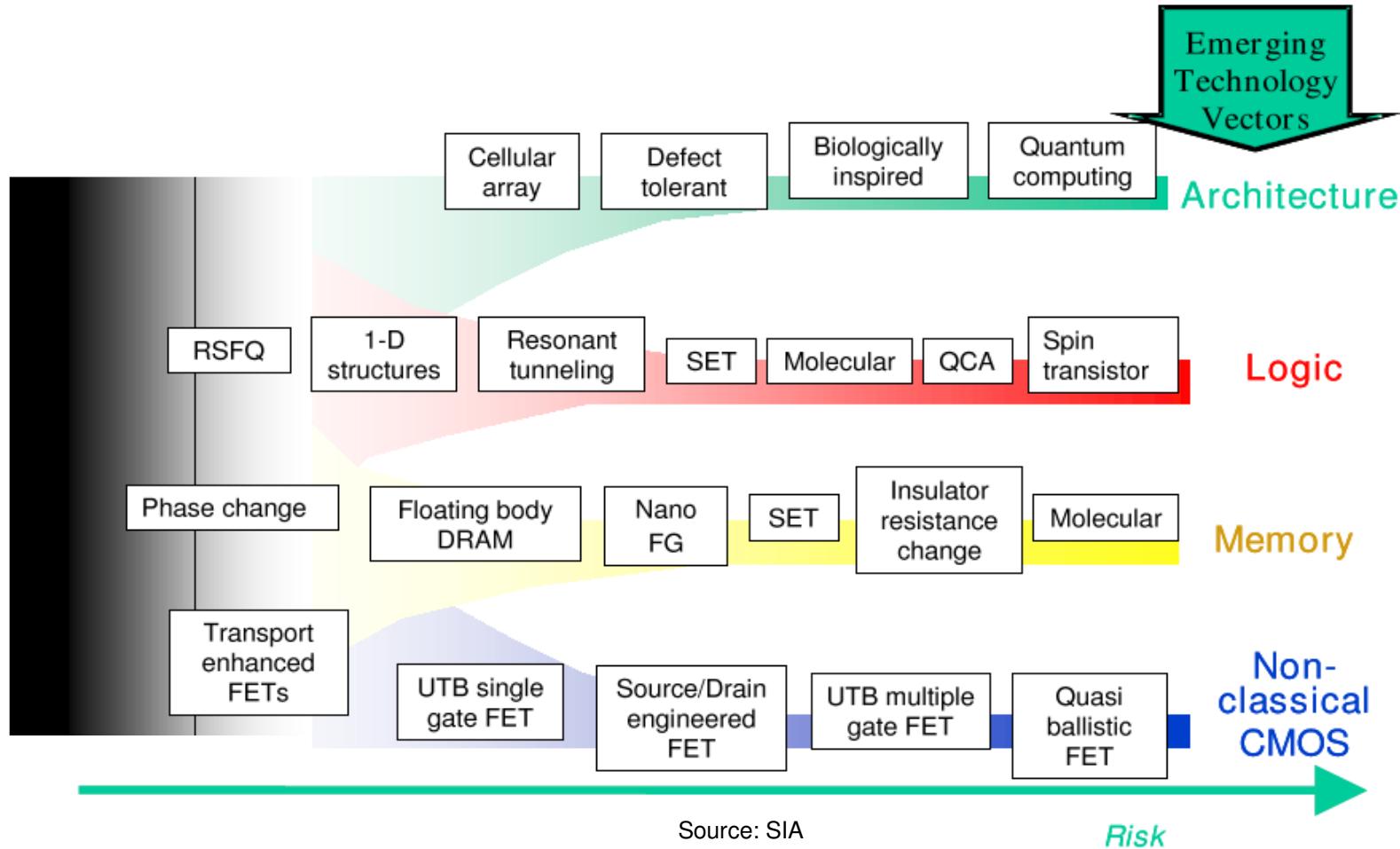


Source : ITRS 2009

Emerging Technology Sequence



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Emerging Research Logic Devices

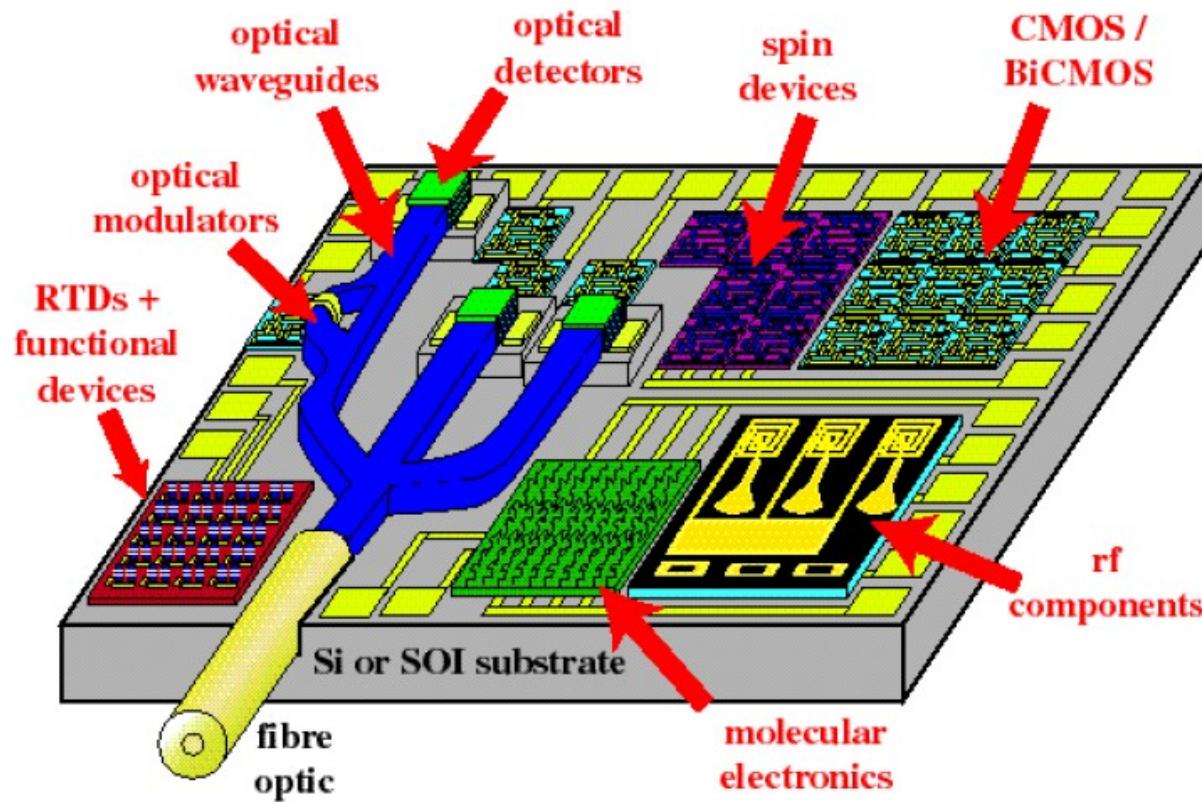


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Device								
	FET	RSFQ	1D structures	Resonant Tunneling Devices	SET	Molecular	QCA	Spin transistor
Cell Size	100 nm	0.3 μ m	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
Density (cm^{-2})	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
Switching Energy, J	2×10^{-18}	$>1.4 \times 10^{-17}$	2×10^{-18}	$>2 \times 10^{-18}$	$>1.5 \times 10^{-17}$	1.3×10^{-16}	$>1 \times 10^{-18}$	2×10^{-18}
Binary Throughput, GBit/ns/cm ²	86	0.4	86	86	10	N/A	0.06	86

Source: SIA

Next generation SoC ?



Going to nanoelectronics

- Do not focus just on the technology
- Features of nanotechnology are slowly integrated into silicon processes
- For technologies under 32nm, interconnections between different levels in the design process must be considered
- Influence on vertical disintegration of semiconductor industry (e.g. fabless companies)

Outline



- Status of the electronics industry
- Research overview @ MES
- System Design
- Strategic research directions
 - Smart Grids
 - Healthcare
 - Adaptronics
- Making the world “smart”, reliable and energy-efficient Wireless sensor networks

The Microelectronic Systems Design Group



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Institut für Datentechnik



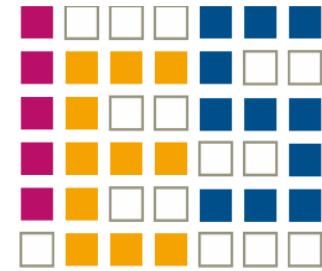
Prof. Dr. Dr. h.c. mult. Manfred Glesner

Prof. Emeritus for Microelectronic Systems



Prof. Dr.-Ing. Klaus Hofmann

Fachgebiet Integrierte
Elektronische Systeme



The Microelectronic Systems Design Group



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- One Post-Doctoral researcher
 - Faizal Samman
- Seven Ph.D.candidates
 - Hans-Peter Keil
 - Leandro Möller
 - Sebastian Pankalla
 - François Philipp
 - Christopher Spies
 - Ping Zhao
 - Pongyupinpanich Surapong
- Three external Ph.D. candidates
 - Kurt Ackermann
 - Enkbold Ochirsuren
 - Elvio Dutra e Silva

Research areas



➤ Application-specific Reconfigurable Logic

- Reconfiguration methodologies
- Reconfigurable processors
- Flexible Wireless Sensor Networks (WSN)
- Energy-efficient reconfigurable architectures

➤ Network-on-Chip Design

- System-on-Chip (SoC) architectures
- NoC topologies and router architectures
- Deadlock-free and adaptive routing strategies

➤ System-Level Design

- Abstract system models for complex SoCs
- Models of computation
- Actor-oriented design
- Multimedia Platforms

➤ Printed Electronics

- Modelling of RFID systems
- Mixed signal design for printed RFID applications
- Device modelling based on new organic and inorganic materials

➤ Wireless Sensor Networks

- Hardware architectures
- Energy Harvesting
- Design Methodology

➤ Adaptronics

- Microelectronic Systems for Structural Health Monitoring
- Lifecycle Engineering

➤ RF and Mixed Signal Circuit Design

- RFID Power Harvester
- RF CMOS circuit design
- Reconfigurable Mixed-Signal Circuits

Currently Running Projects



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- TUD-Merck Labor: *Printed Electronics*



- BMBF-Exzellenzinitiative: „*Da Vinci*“

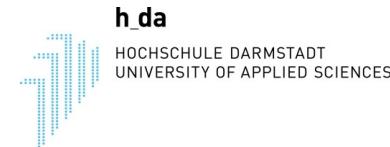
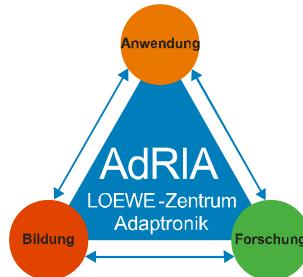


Currently Running Projects



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- LOEWE AdRIA: *Adaptronik*



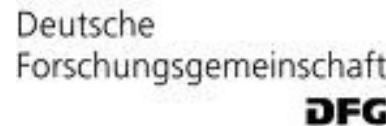
LOEWE – Landes-Offensive
zur Entwicklung Wissenschaftlich-
ökonomischer Exzellenz

- EU FP7 MoDe: *Wireless Sensor Networks*



Currently Running Projects

- DFG Project: *Multiprocessor System-on-Chip Design (in cooperation with Dr.-Ing. Leandro Indrusiak, Lecturer at York University)*



- GSI: *Reconfigurable Real-Time Control Systems (LOEWE-FAIR follow-up Project)*



DFG Graduate School for Computation Engineering

Current International Academic Cooperations



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- Mongolian University of Sciences and Technology (MUST)
- University of Melbourne (Prof. Saman Halgamuge)
- University of Sydney (Prof. Philip Leong)
- Montpellier Laboratory of Informatics, Robotics, and Microelectronics (LIRMM)
- Tallinn University of Technology (CREDES + CEBE)
- York University (Dr.-Ing. Leandro Soares Indrusiak)
- University of Bucharest

-
- INPG/TIMA in Grenoble (Frankreich)**
- Stanford University (USA)**
- Georgia Tech (USA)**
- Ohio University (USA)**
- Virginia Tech (USA)**
- University of Central Florida (USA)**
- University Politehnica of Bucharest (Rumänien)**
- King Saud University (Kingdom of Saudi Arabia)**
- UFRGS Porto Alegre (Brasilien)**
- CINVESTAV-Institut Mexico City (Mexiko)**
- University of Lyngby (Dänemark)**
- University of Linköping (Schweden)**
- Tallinn University of Technology (Estland)**
- Kaunas University (Litauen)**
- Mongolian Technical University (Ulaanbaatar)**
- Zhejiang University (China)**
- Fudan University, Shanghai**
- CUHK, Hong Kong**
- CMC, Kingston**
- ALARI, Lugano**
- Slovak Academy of Sciences**
- Silesian University of Technology**
- KTH Stockholm**
- INESC, Lisbon**
- IMEC, Leuven**
- University of Sfax**
- Politecnico de Milano**
- Melbourne University**
- CEERI, Pilani**
- TU Delft**
- TU Eindhoven**
- TU Iasi, Romania**
- PUC Peru, Lima**
- EPFL, Lausanne**
- University of Crete**
- KAIST, Daejeon**
- TU Wien**
- TU Budapest**
- CINVESTAV, Mexico**
- University of Sharjah**
- NCKU, Tainan**
- Tampere University of Technology**
- TU Gdansk**
- University of Maribor**

Research overview



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- Organic and Printed Electronics
- RFID Circuit Design
- Crossbar switches
- Hardware architectures for Image Processing
- GSI, FAIR
- Design Space Exploration of Wireless Sensor Networks
- Network on Chip

Printed Electronics at TUD-MES



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▪ Printed Electronics at TUD-MES

• MerckLab

- Cooperation between TUD and Merck KGaA
- Partners of the TUD:
 - Prof. Glesner (MES)
 - Prof. Dörsam (IDD)
 - Prof. Rehan (DKI)
 - Prof. Schneider (Inorganic Chemistry)
 - Prof. Rödel (Material Science – Nonmetallic-Inorganic materials)
 - Prof. von Seggern (Material Science – Electronic materials)
 - Prof. Jägermann (Material Science – Surface science)



- Printed Inorganic Electronic for RFID applications

• Polytos

- Printed Organic Electronics
- Partners:
 - TUD, BASF, Merck KGaA, PolyIC, SAP, Bosch, Heidelberger Druck...
- Smart Labels



DaVinci BMBF Excellenzcluster: Forum Organic Electronics



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- Printed Electronics at TUD-MES
 - Polytos

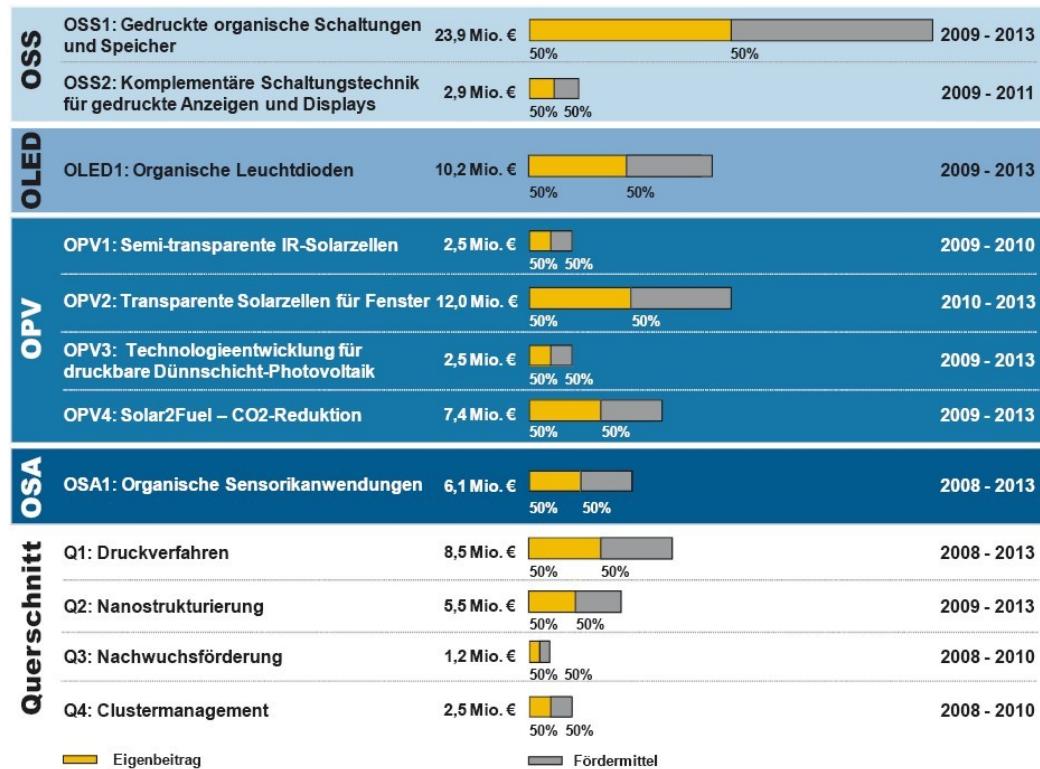
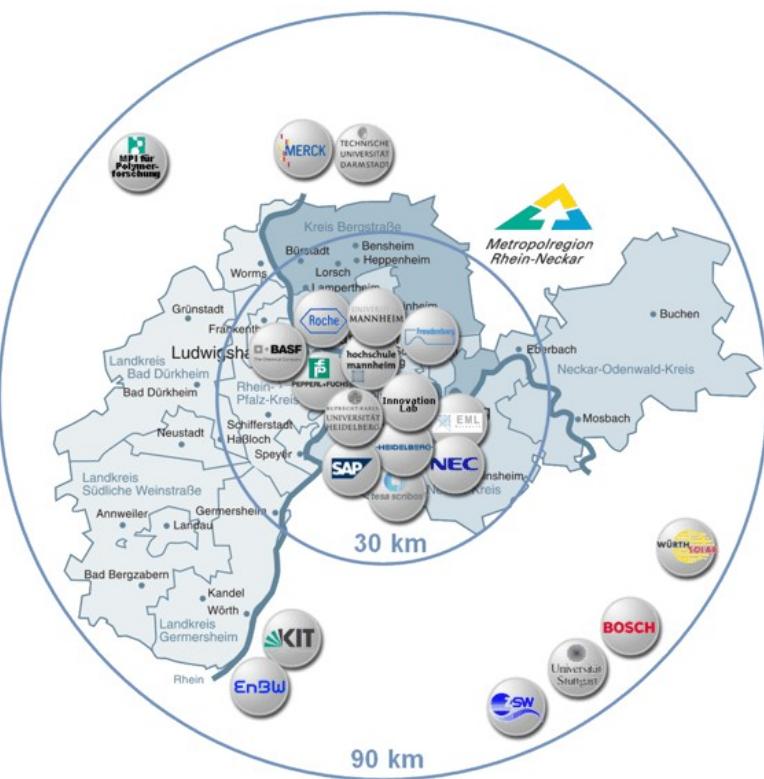
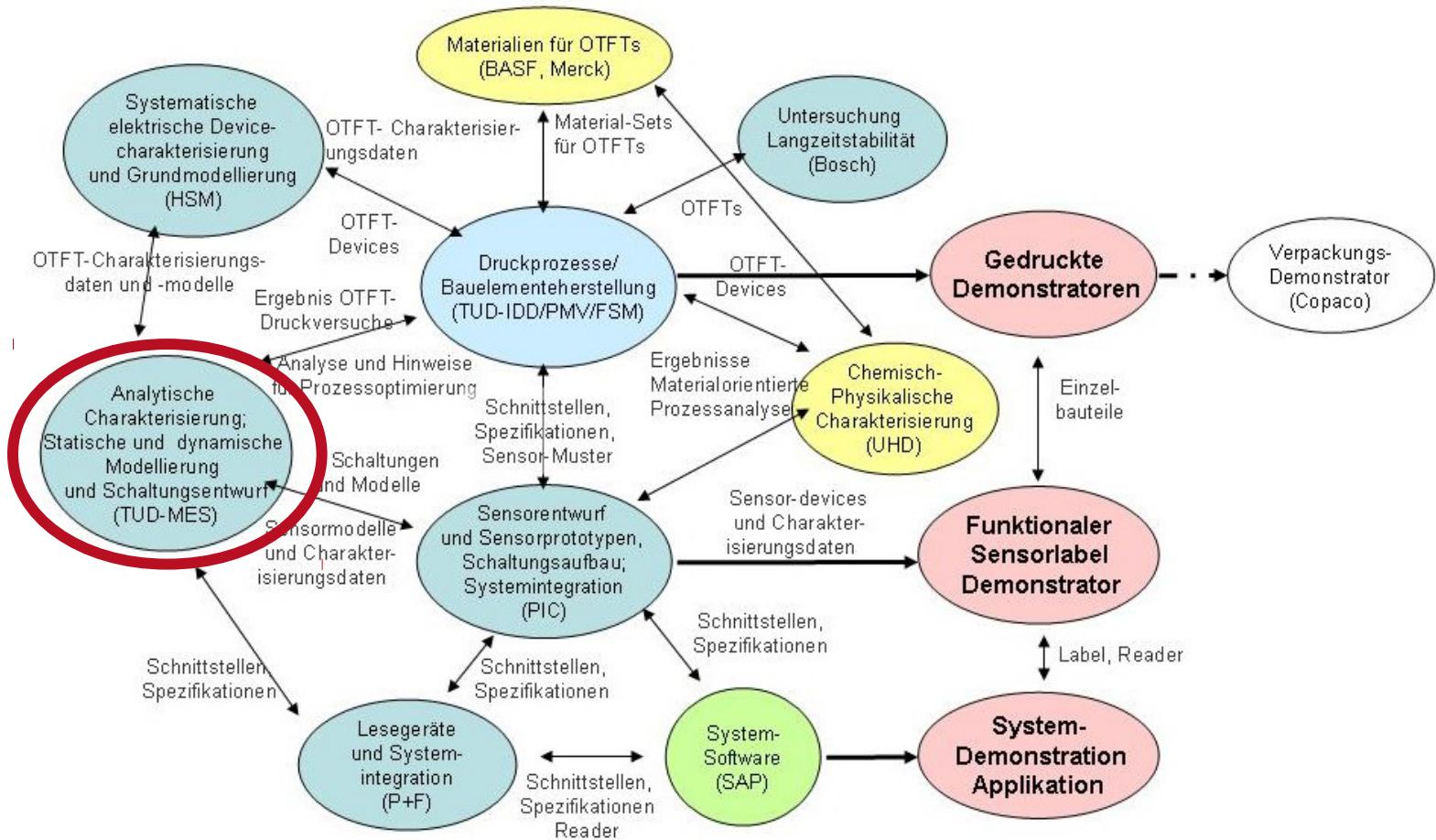
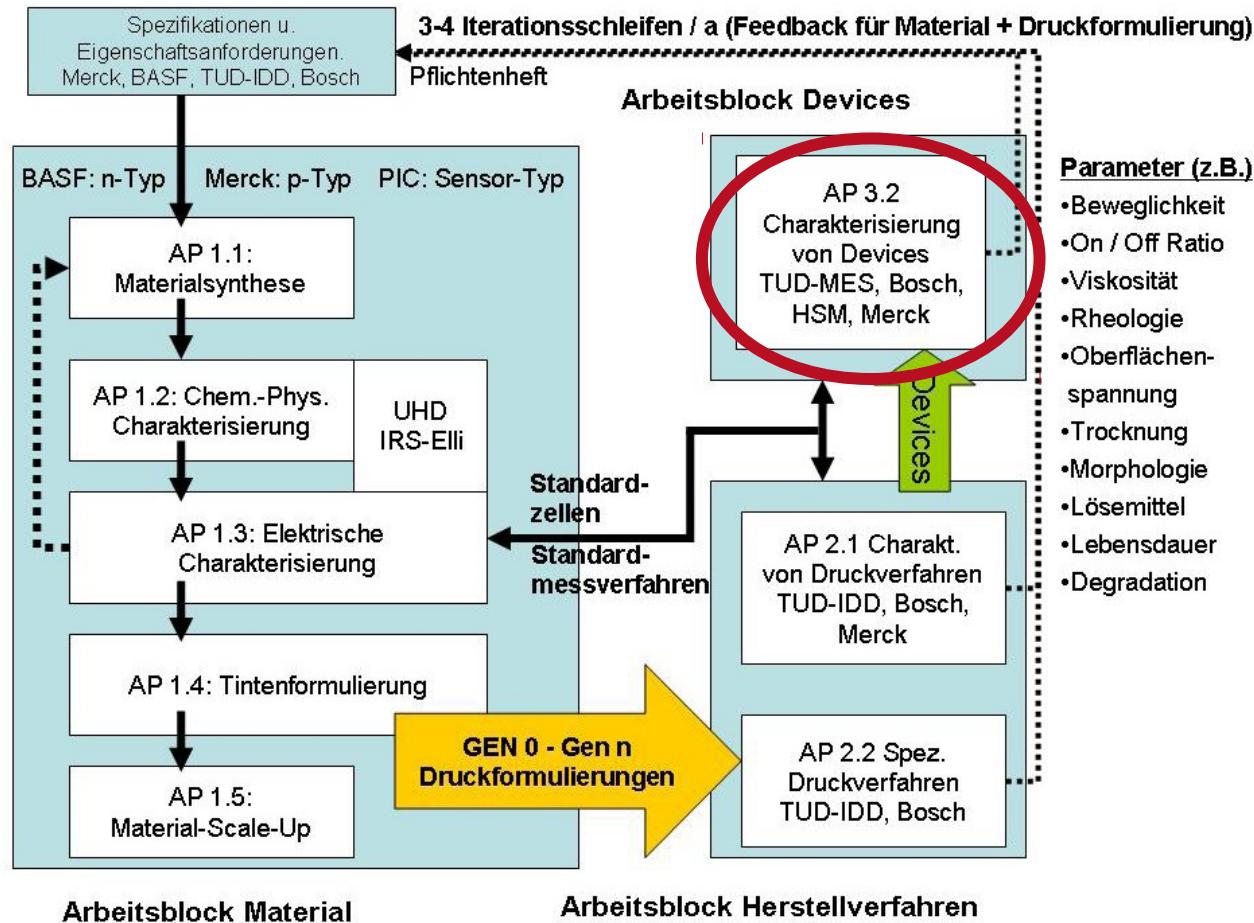


Abb. 14: Übersicht der Projekte

Competences and cooperation between partners



Work division between the partners



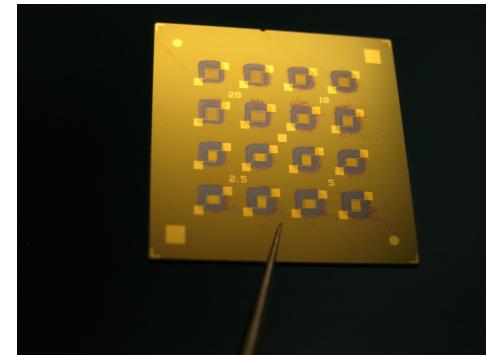
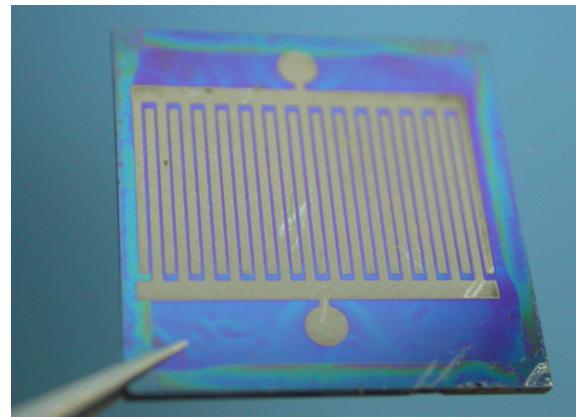
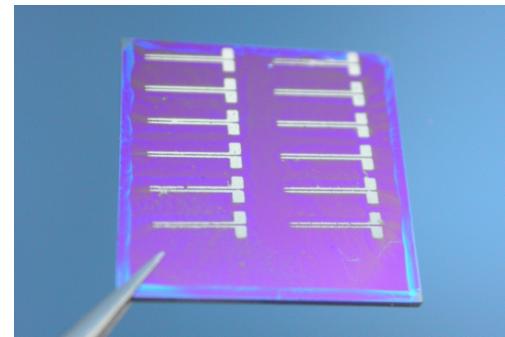
Expertise of TUD-MES

- TUD-MES has expertise for many years in development of circuits for classical silicon-based CMOS transistors
- First generations of CAD-tools in Europe were developed at TUD-MES
- Research on methods for development of complex integrated systems-on-chip
- Within the MerckLab, TUD-MES worked on RFID-chips:
 - Characterisation of printed inorganic transistors
 - Expertise in building new measuring set-ups for organic TFTs
 - New material system for active layer was developed
 - Building up a environment for simulation of RFID-tags

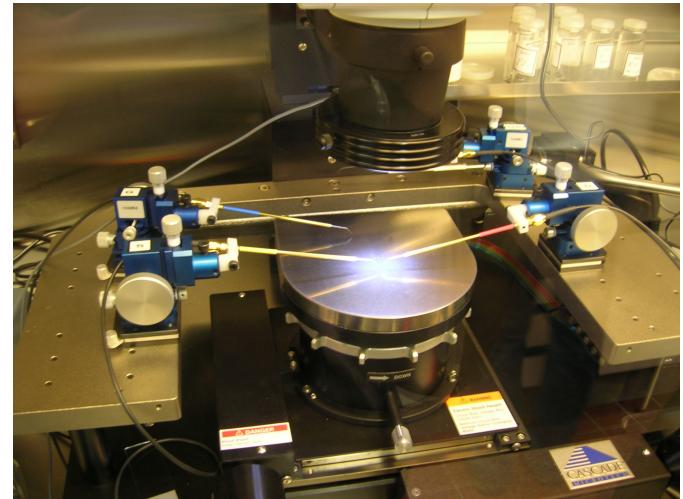
- Printed Electronics at TUD-MES
 - MerckLab -printing inorganic materials
 - Silver - Ink
 - Dielectrics
 - ZnO-precursor



Transparent Precursor solution



- Printed Electronics at TUD-MES
 - Measurement Setup
 - Characterisation of semiconducting, dielectric and conducting materials





Contact



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RFID Air Interface Standards - ISO/IEC 18000



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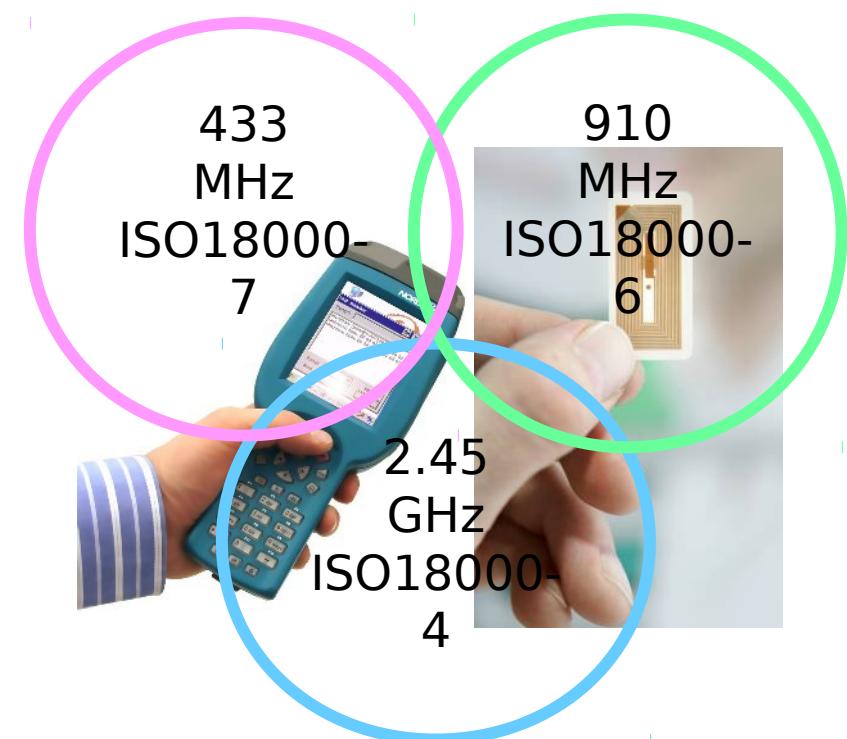
- ISO/IEC defines a series of RFID air interface standards from 18000-1 to 18000-7 for item identification world.
- A diversity of RFID specifications is regulated:
 - Multi-standard: several frequency bands have been assigned to RFID applications, such as 125KHz, 13.56MHz, 433MHz, 910MHz and 2.45GHz.
 - Multi-mode: Each frequency band has an individual parameter definition.



RFID: Prospective Future

The need of having a platform capable of multiple standard operation becomes obvious in order to:

- take advantage of different frequency bands
- increase of the compatibility of RFID systems
- reduce manufacturing costs



Source: NORDICID

Challenges in RFID



The principle challenges are:

- to limit the additional hardware with more integrated functionality
- to reuse the common blocks between different frequencies and modes of operation

Frequency agile RFID systems are proposed to include **tunable microwave frontends** with characteristics as:

- Adjustable resonant frequency, impedance and phase delay are controlled by a DC voltage.
- High permittivity material in order to reduce size
- Passively tunable in combination with ultra low power.

Frequency Agile RFID Systems



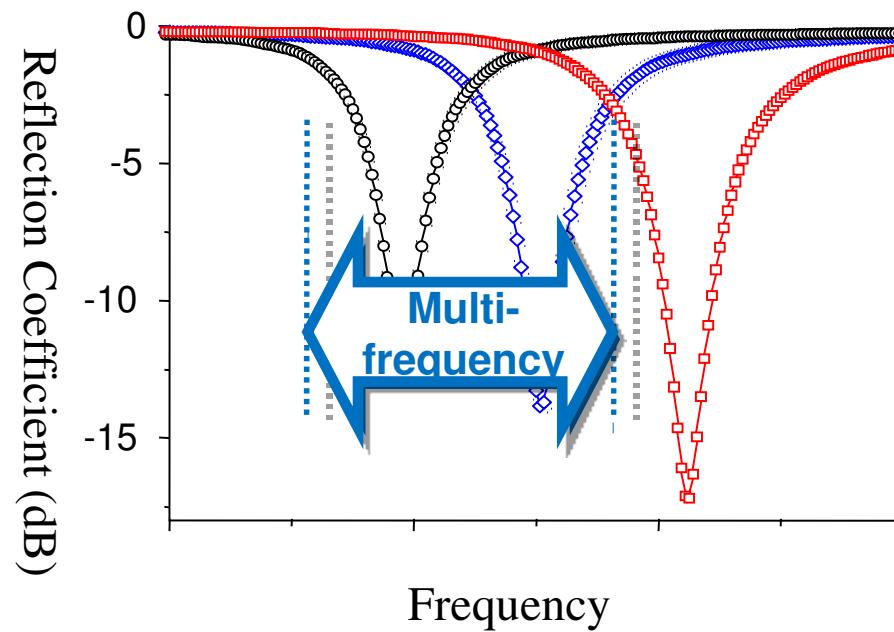
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- Tunable matching networks guarantee the power harvesting efficiency over multiple frequency bands. It also **stabilizes the load** for more reliable transmission, e.g. when the consumed current varies.

Frequency Agile RFID Systems



- An antenna loaded with varactors can cover a wide frequency range within the same antenna dimension. The target bands are 433MHz, 910MHz and 2.45GHz.



Contact



M. Sc. Ping Zhao

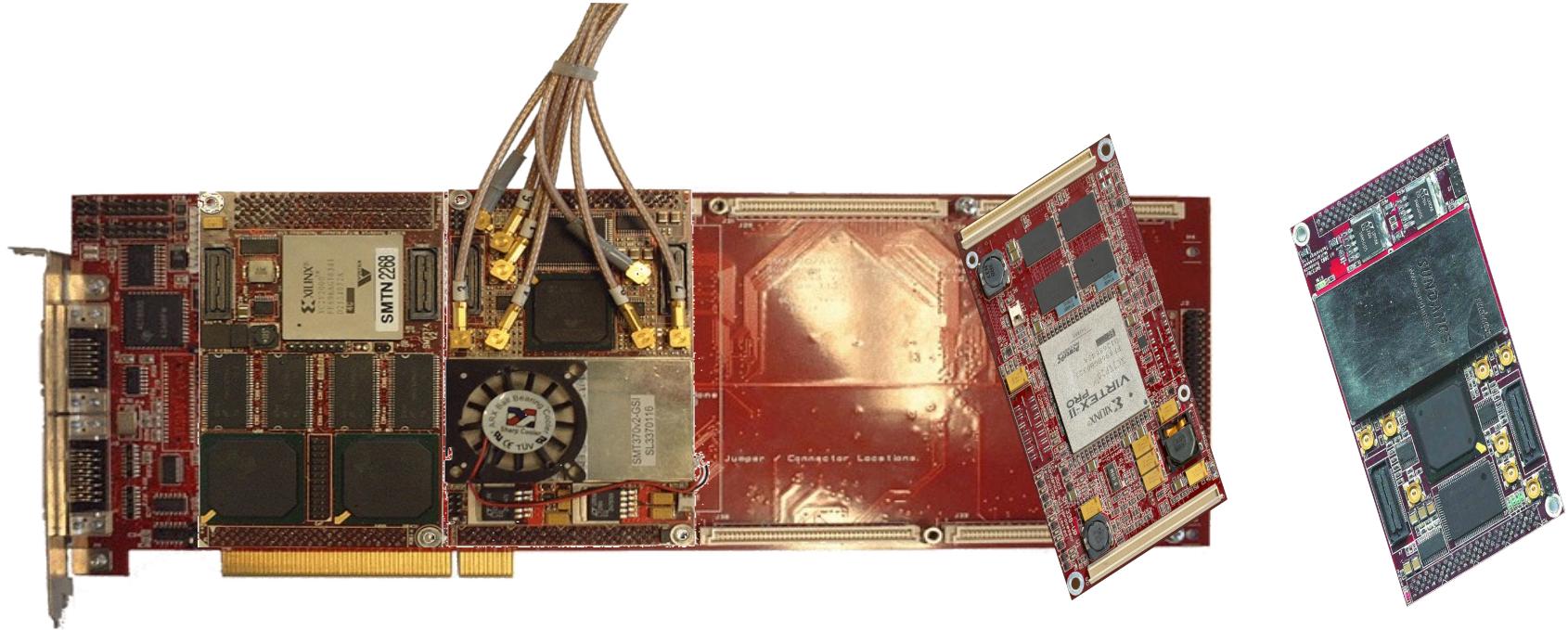
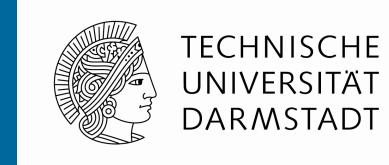
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Design and Analysis of High-Speed Switch Structures for High-Bandwidth Digital Systems



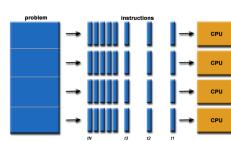
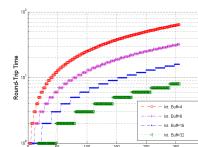
Objective



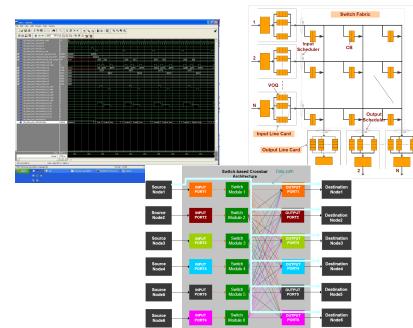
Considering on High-Speed interconnection structures for parallel and real-time embedded system applications comprised of:

- Design and analysis of bus-based and Switch-based architectures
- Fast and efficient Scheduling algorithms
- Novel service mechanisms to improve Quality-of-Service (QoS)
- Simpler hardware structures for Silicon-based and FPGA-based

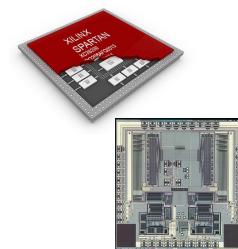
```
 Mechanism - Round Robin based scheduling mechanism
 Input - Credit Rules (Ci,j), Request (Ri,j), service rate (Servicei)
 Output - Priority (Pi,j), requester, start, enable, ...
 1) Initialize all credits to zero
 2) while (!done)
    3)   for (j = 0; j < N; j++)
        4)     if (start[j] == 1)
            5)       enable[j] = 1
            6)       counter[j] = 1
            7)       if (counter[j] > max)
                8)         break
            9)       if (enable[j] == 1)
              10)         if (Ri,j > 0)
                  11)           if (Servicei > Ri,j)
                      12)             Ri,j = 0
                      13)             counter[j] = 0
                      14)             enable[j] = 0
                      15)             start[j] = 0
                      16)             if (Ri,j > 0)
                          17)               Servicei = Ri,j
                          18)               Ri,j = 0
                          19)             else
                            20)               Servicei = Ri,j
                            21)               Ri,j = Ri,j - Servicei
                          22)             counter[j] = 1
                          23)             enable[j] = 1
                          24)             start[j] = 1
                          25)             if (Servicei > Ri,j)
                              26)               Ri,j = 0
                              27)               counter[j] = 0
                              28)               enable[j] = 0
                              29)               start[j] = 0
                          30)             else
                            31)               Servicei = Ri,j
                            32)               Ri,j = Ri,j - Servicei
                          33)             counter[j] = 1
                          34)             enable[j] = 1
                          35)             start[j] = 1
                          36)             if (Servicei > Ri,j)
                              37)               Ri,j = 0
                              38)               counter[j] = 0
                              39)               enable[j] = 0
                              40)               start[j] = 0
                          41)             else
                            42)               Servicei = Ri,j
                            43)               Ri,j = Ri,j - Servicei
                          44)             counter[j] = 1
                          45)             enable[j] = 1
                          46)             start[j] = 1
                          47)             if (Servicei > Ri,j)
                              48)               Ri,j = 0
                              49)               counter[j] = 0
                              50)               enable[j] = 0
                              51)               start[j] = 0
                          52)             else
                            53)               Servicei = Ri,j
                            54)               Ri,j = Ri,j - Servicei
                          55)             counter[j] = 1
                          56)             enable[j] = 1
                          57)             start[j] = 1
                          58)             if (Servicei > Ri,j)
                              59)               Ri,j = 0
                              60)               counter[j] = 0
                              61)               enable[j] = 0
                              62)               start[j] = 0
                          63)             else
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                          69)             if (Servicei > Ri,j)
                              70)               Ri,j = 0
                              71)               counter[j] = 0
                              72)               enable[j] = 0
                              73)               start[j] = 0
                          74)             else
                            75)               Servicei = Ri,j
                            76)               Ri,j = Ri,j - Servicei
                          77)             counter[j] = 1
                          78)             enable[j] = 1
                          79)             start[j] = 1
                          80)             if (Servicei > Ri,j)
                              81)               Ri,j = 0
                              82)               counter[j] = 0
                              83)               enable[j] = 0
                              84)               start[j] = 0
                          85)             else
                            86)               Servicei = Ri,j
                            87)               Ri,j = Ri,j - Servicei
                          88)             counter[j] = 1
                          89)             enable[j] = 1
                          90)             start[j] = 1
                          91)             if (Servicei > Ri,j)
                              92)               Ri,j = 0
                              93)               counter[j] = 0
                              94)               enable[j] = 0
                              95)               start[j] = 0
                          96)             else
                            97)               Servicei = Ri,j
                            98)               Ri,j = Ri,j - Servicei
                          99)             counter[j] = 1
                          100)            enable[j] = 1
                          101)            start[j] = 1
                          102)          endfor
                          103)        endfor
                          104)      endwhile
                          105)    endfunction
```



**System design
& Analysis**



**Hardware design
& verification**



**FPGA-based
& Silicon-based**

Crossbar Interconnection



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M. Eng. Pongyupinpanich Surapong

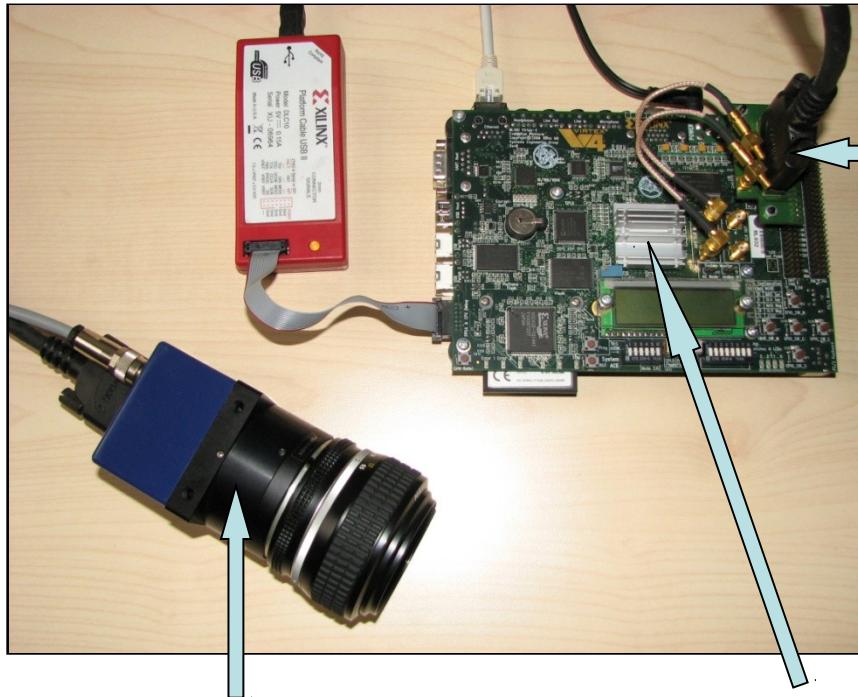
surapong@mes.tu-darmstadt.de

Microelectronic Systems Design Group

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Tel: +49 (0) 6151 16 - 4337

Self-reconfigurable hardware for digital image processing



CMOS Camera (B/W):
2048 x 2048 pixels
15 frames/sec.

Xilinx ML-402 Eval.-Board:
Virtex-4 SX35 FPGA
64 MB DDR2-SDRAM
9Mb SRAM



Standardized camera-link
connector

Self-reconfigurable hardware for digital image processing



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- Global goals:
 - Short time-to-market
 - Merging performance and flexibility
 - Providing abstraction methods to reduce the design-complexity
 - Intuitive specification of the desired functionality
- Research:
 - Design-Automation
 - Direct specification of the processing pipeline
 - Library based approach
 - Minimizing design-times and adaption durations
 - High degree of technology independency
 - FPGA-based self-reconfigurable architectures
 - Resource efficiency
 - Enhanced access to reconfiguration resources
 - Minimization of reconfiguration costs (slot-alternating execution)

Self-reconfigurable hardware for digital image processing



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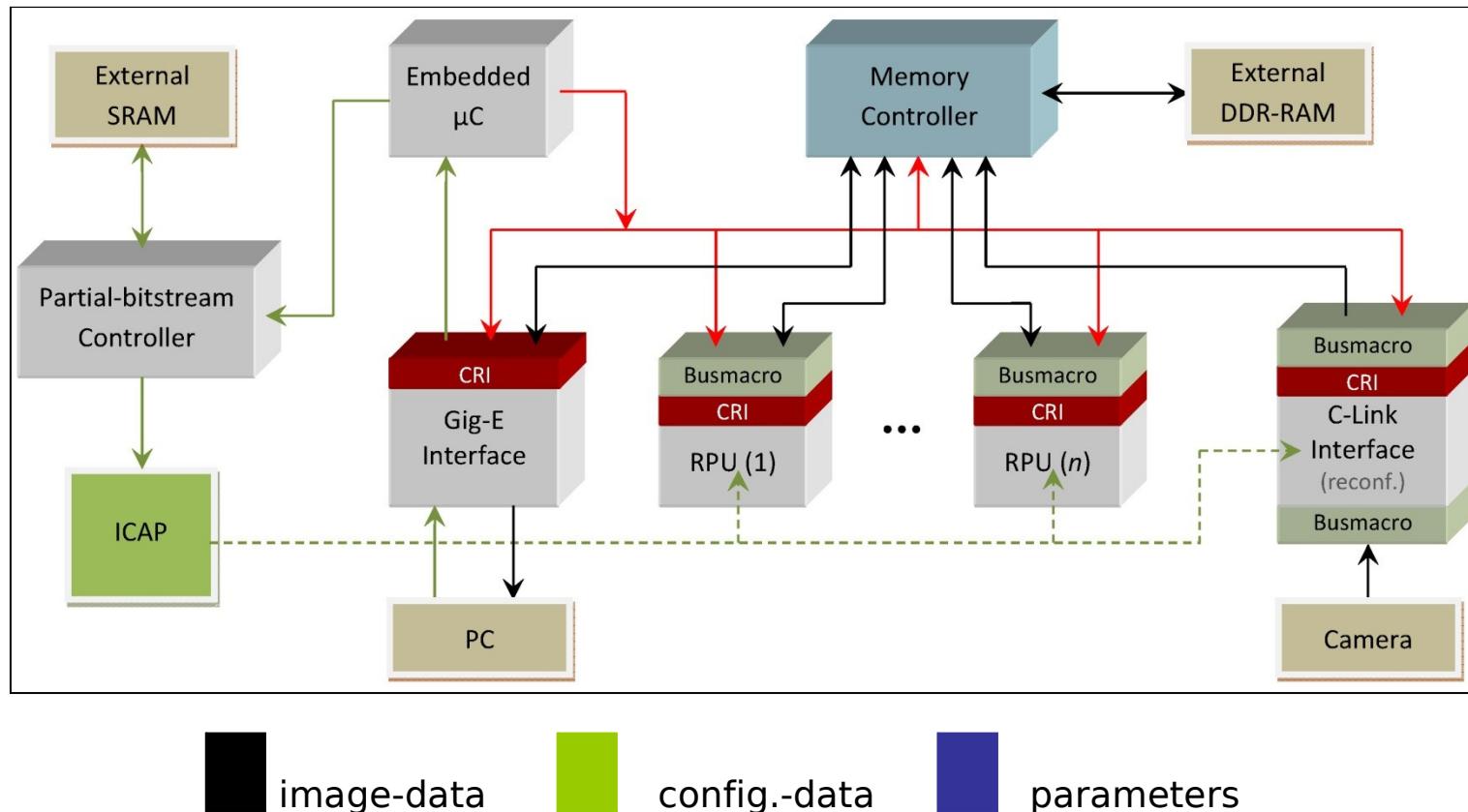
- Research (continue):
 - Concept of a self-reconfigurable frame-grabber
 - Standardized high-speed interfaces to cameras and PC
 - Integration of the optimised reconfiguration infrastructure
 - **Memory-centric topology**
 - Efficient domain-specific memory management
 - **Reduction of required communication primitives (bus macros), reducing signal propagation delays**
 - Abstraction of memory management services, simplifying the design of IP-Cores
 - Infrastructure for dynamic parameterisations of components
 - Results:
 - Achieving the max. reconfiguration bandwidth of the device (reduction of reconfiguration times up to 99,6%)
 - Hiding remaining reconfiguration and parameterisation times
 - Reduction of memory related bus macro primitives up to 85%, keeping the overall latency costs below 1,5%.

Self-reconfigurable hardware for digital image processing



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Structure of the self-reconfigurable frame-grabber



Self-reconfigurable hardware for digital image processing



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Contact

Dipl.-Ing. Kurt Ackermann

kurt.ackermann@vitronic.com



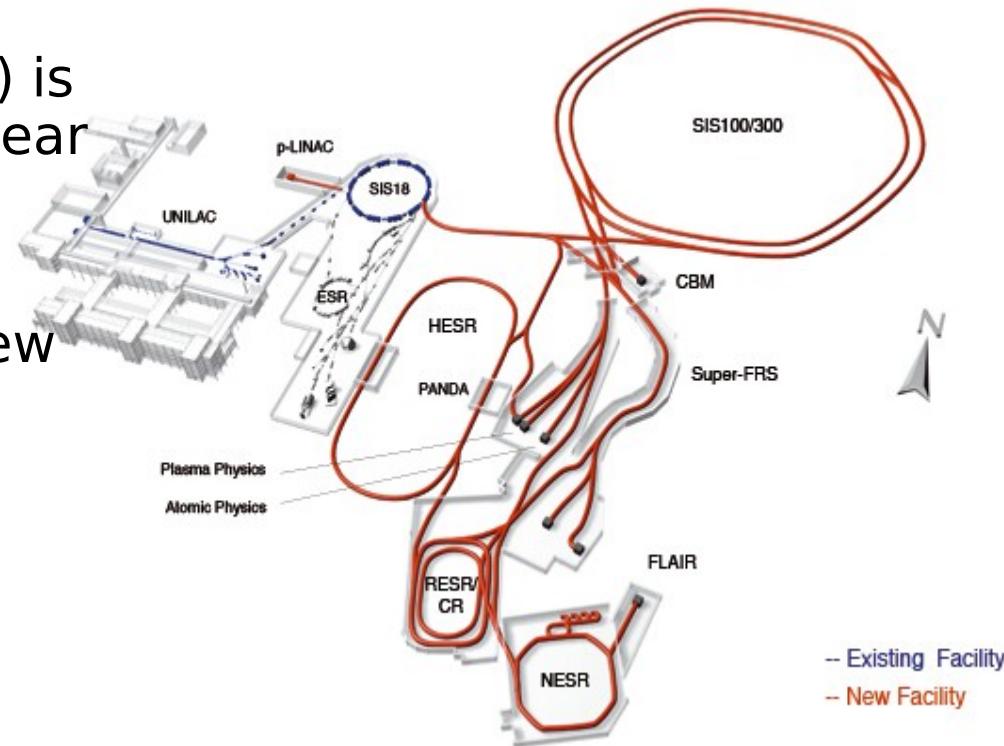
www.vitronic.de

Design Space Exploration for a Heavy-Ion Synchrotron

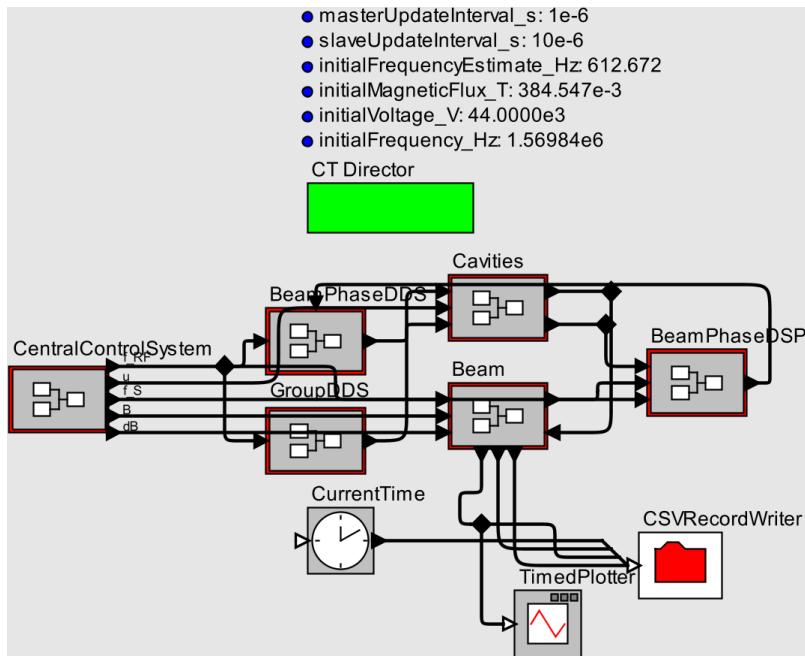


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- The *Gesellschaft für Schwerionenforschung* (GSI) is a nuclear research facility near Darmstadt, Germany
- It is currently extended a new synchrotron, SIS100
- SIS100 will be digitally controlled
 - this enables new features
 - in past projects, digital systems performance was not sufficient



Modelling and Simulation



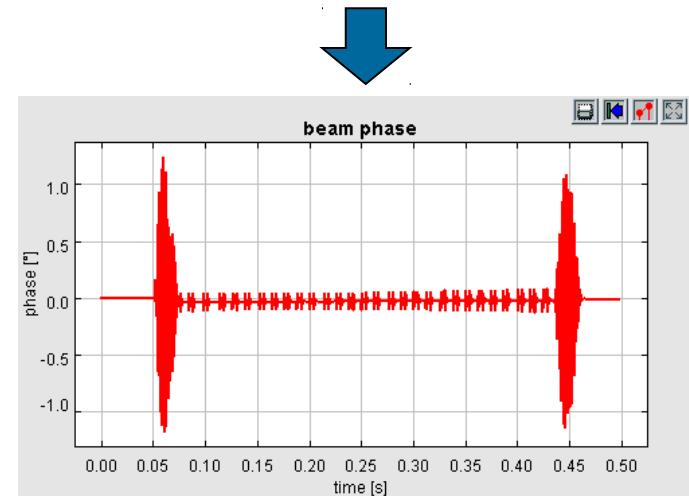
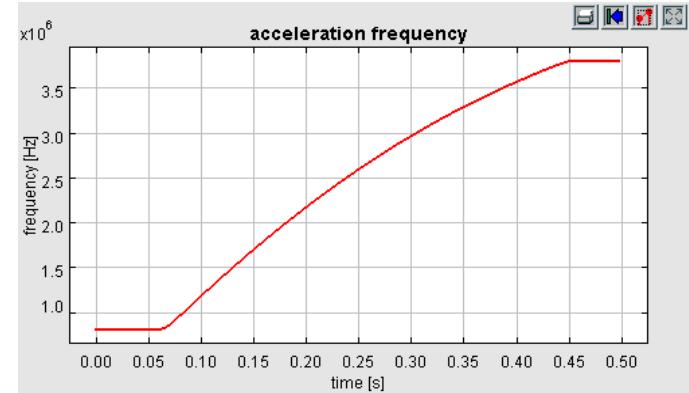
- The accelerator physics, its distributed digital control systems and the communication links between them are jointly modelled
- We use *Ptolemy II* for mixed-signal simulation
- The feasibility of control algorithms can be tested
- Design alternatives (e. g. different sampling rates) can be compared to each other

Results



So far, we produced the following:

- An abstract, parametrized model of the accelerator system
 - including multiple, spatially distributed components
 - including local analog and digital control loops
 - including global digital synchronization control
 - including global beam phase control
 - including a linearized beam model
- Insight into the feasibility of the proposed control algorithms
 - Synchronization and beam phase control work as expected
 - Simulation results are confirmed by experiments



Design Space Exploration for a Heavy-Ion Synchrotron



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System Level Design space exploration of application-specific wireless sensor systems



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- **Objective**

- Propose a tool that can evaluate the alternative designs of wireless sensor system based on SoC hardware, while the hardware is still in its design flow

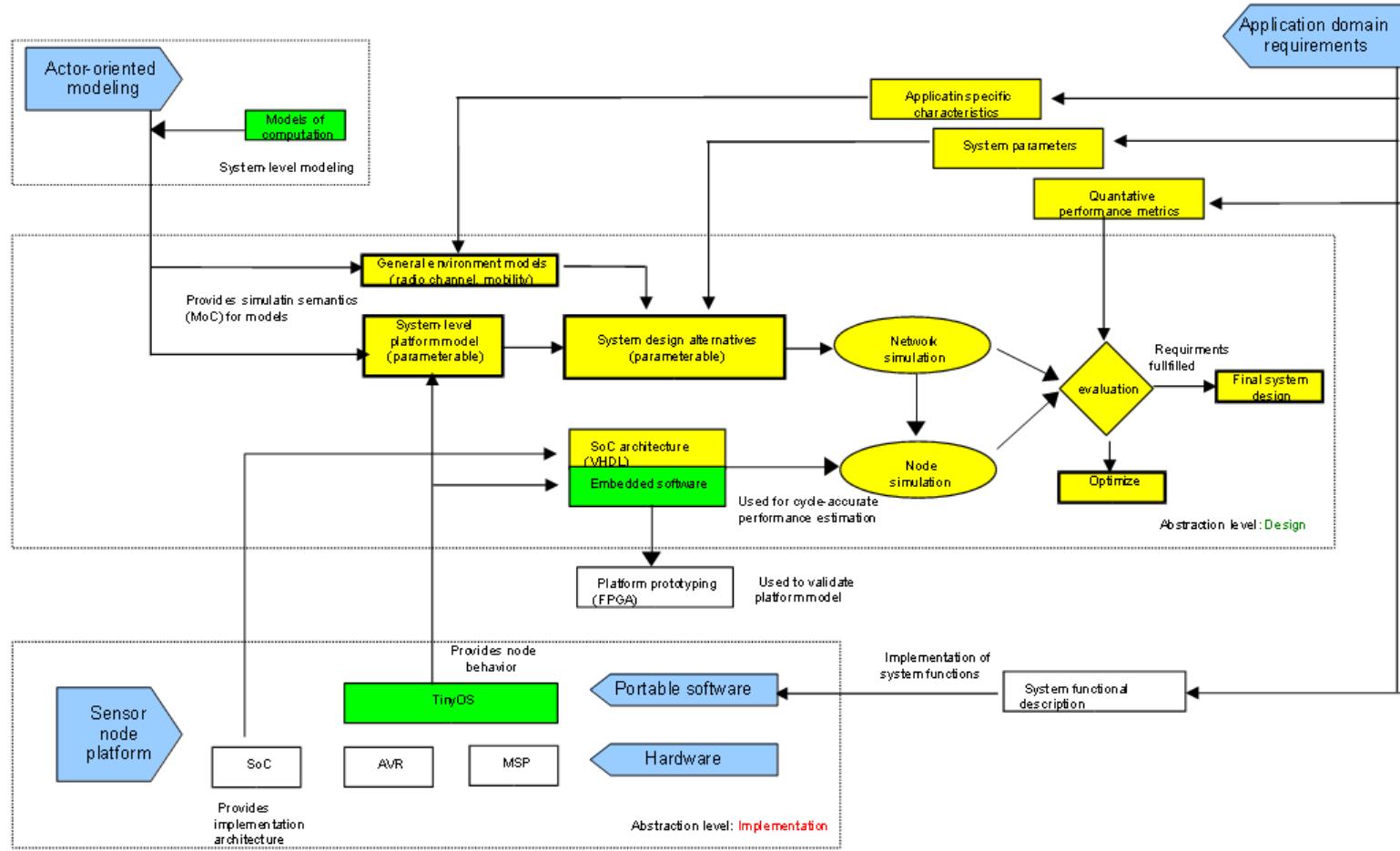
- **Methodological approach**

- Abstract a system in hierarchical levels (node & network)
- Perform network and hardware simulations to obtain performance estimates
- Analysis on the obtained results

- **Levels of abstraction**

- Node : SoC architecture in VHDL, TinyOS sensor software
- Network : Actor models of sensor node platform template, application specific models (radio channel, mobility)

System Level Design space exploration of application-specific wireless sensor systems



Wireless Sensor Networks

Design-Space Exploration



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Contact

M.Sc. Enkhbold Ochirsuren

ochirsuren@efe-gmbh.de

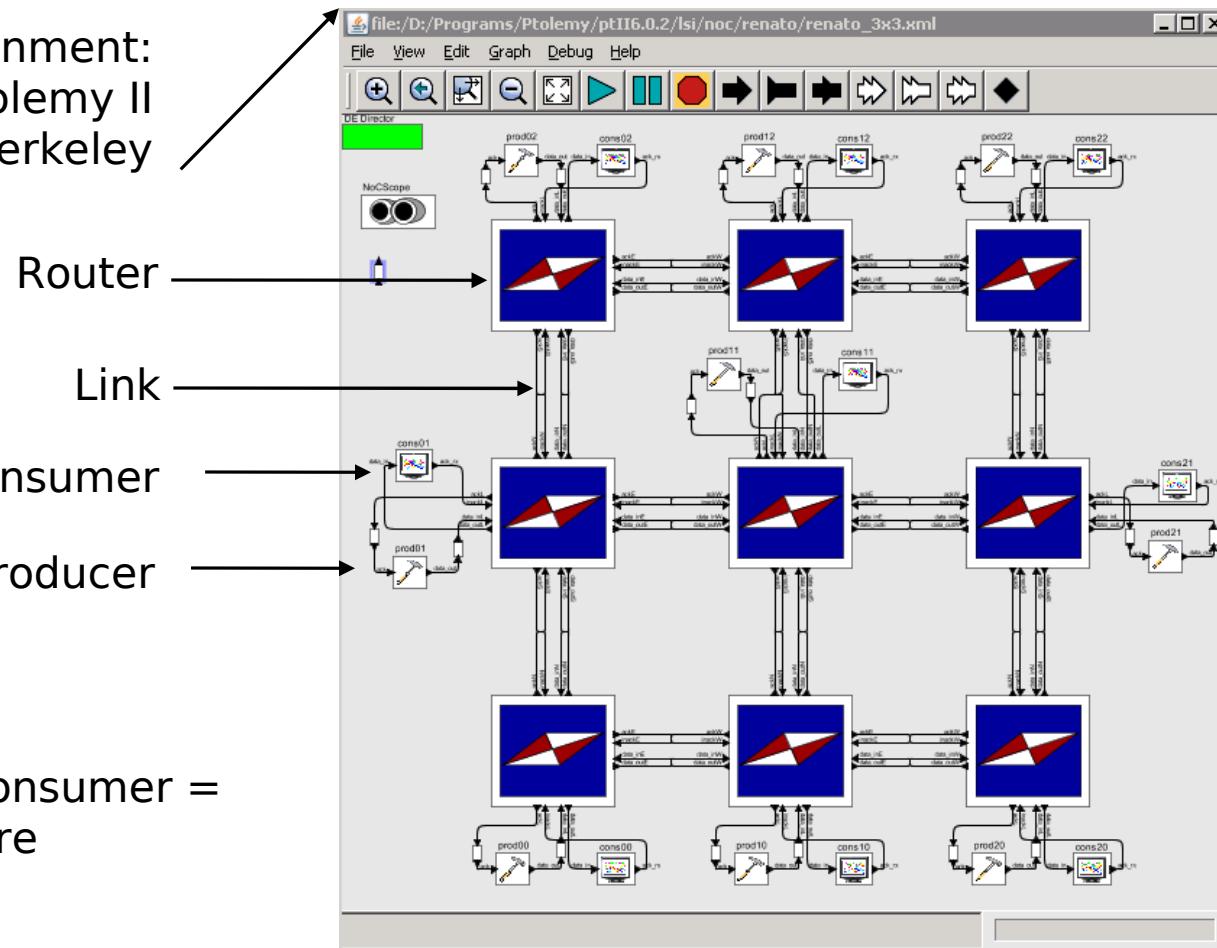


www.efe-gmbh.de

Network-on-Chip High Level Modelling



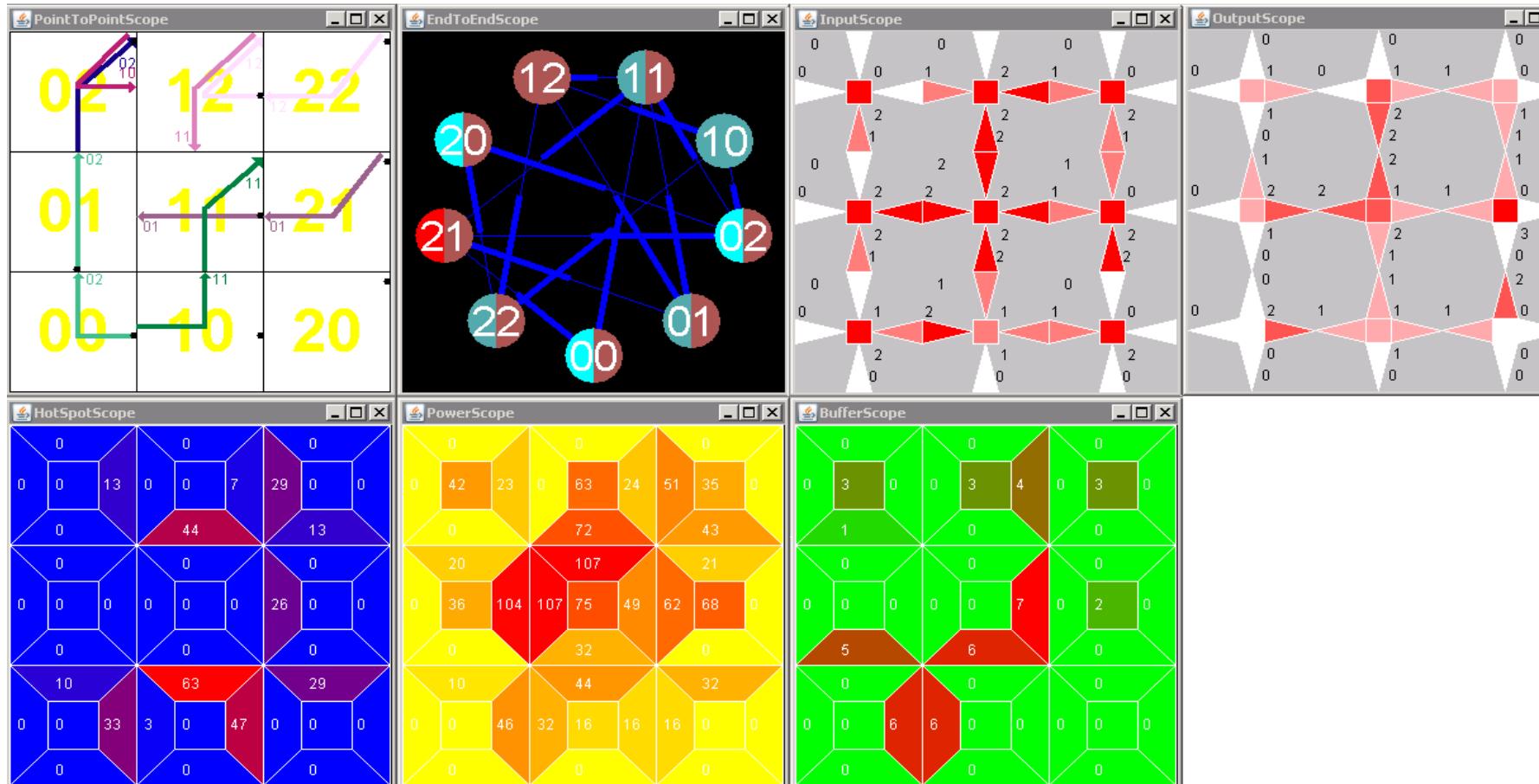
Simulation Environment:
Ptolemy II
From UC Berkeley



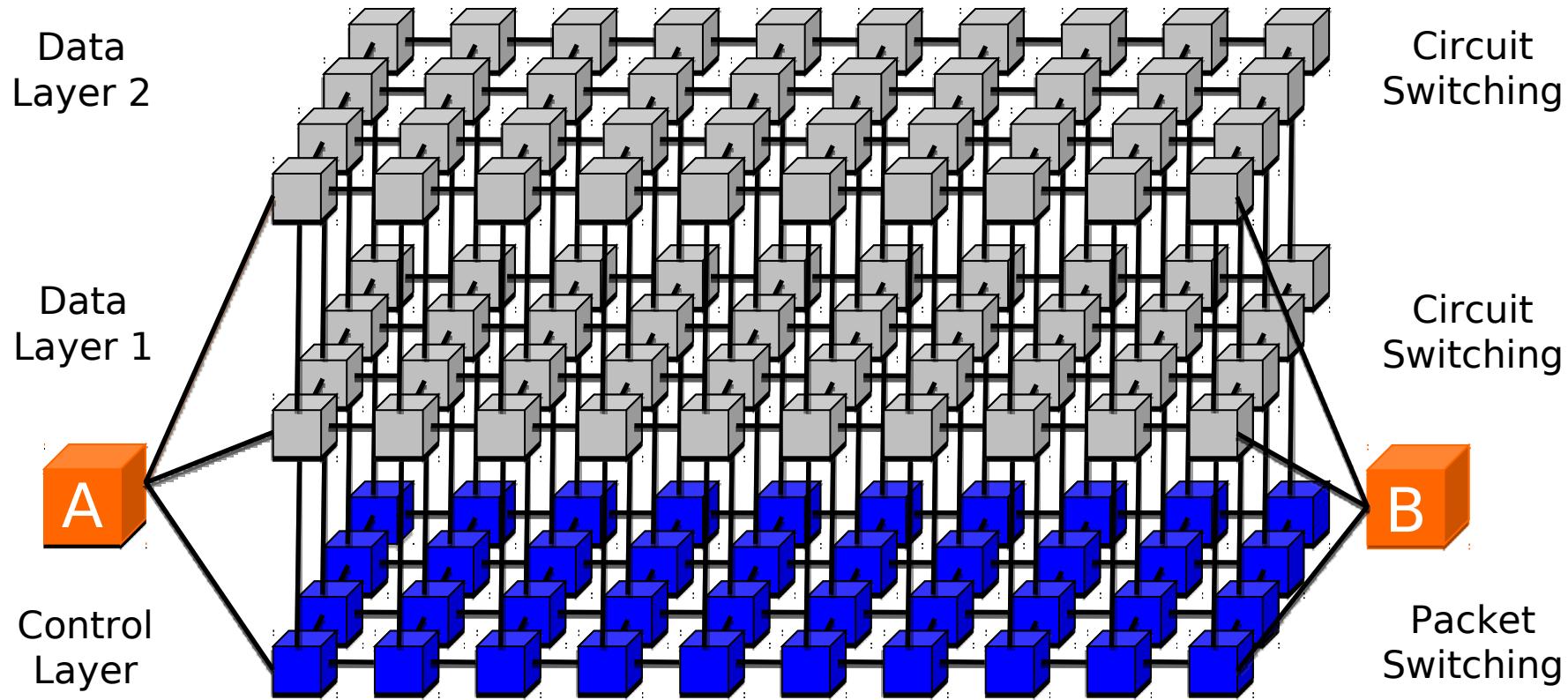
Network-on-Chip Monitoring and Debugging



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Network-on-Chip Multi-Layer Design



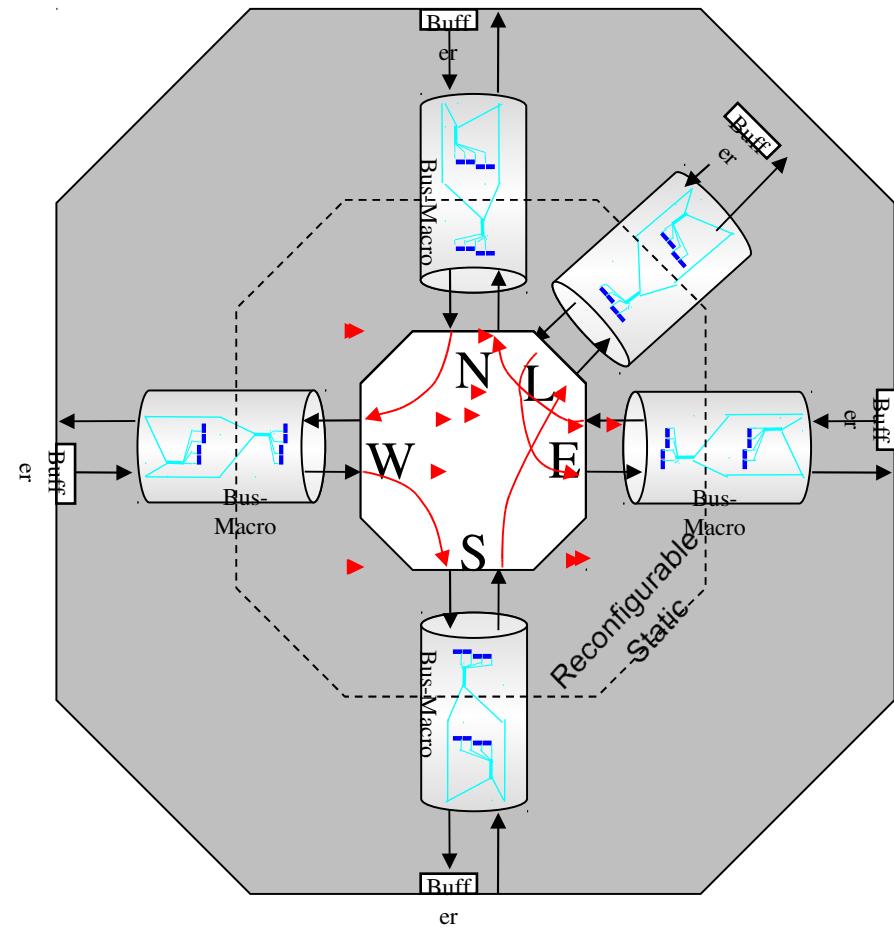
IP Cores have more than one circuit switching network to establish long-term communications

Network-on-Chip Router Partial Reconfiguration



Small area overhead routers since arbitration, routing and crossbars are not implemented on router logic.

This router design is for Xilinx FPGAs.





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Outline



- Status of the electronics industry
- Research overview @ MES
- **System Design**
- Strategic research directions
 - Smart Grids
 - Healthcare
 - Adaptronics
- Making the world “smart”, reliable and energy-efficient Wireless sensor networks

System Design



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- “Increase level of abstraction to improve comprehension about a system and enhance probability of successful implementation of a functionality in a cost-effective manner”

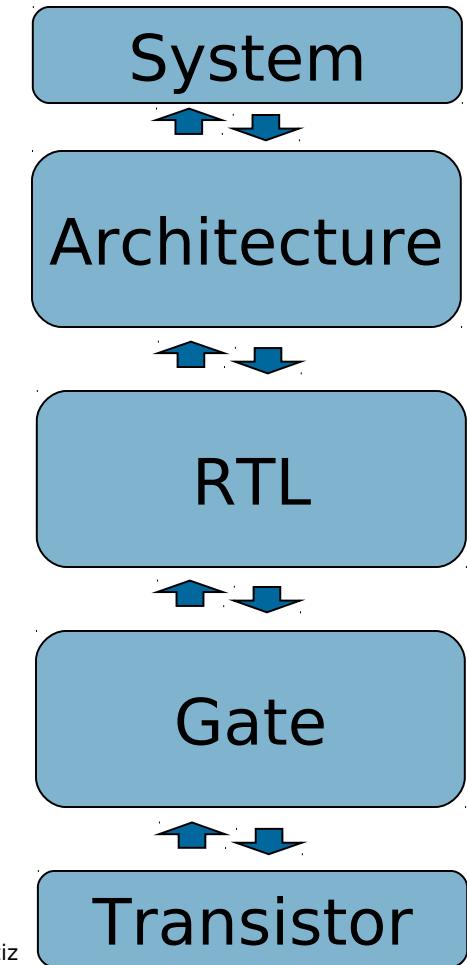
IC Design

Abstraction levels



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- **System**
 - General functionality and structural overview
- **Architecture / Algorithm**
 - View of major blocks (IPs) and their relation
 - Partition Hardware/Software
 - Algorithmic functionality
- **RTL**
 - Functionality at register level
 - Macros of combinational logic
- **Gate**
 - Interconnections of gates
- **Transistor**
 - Detailed physical implementation

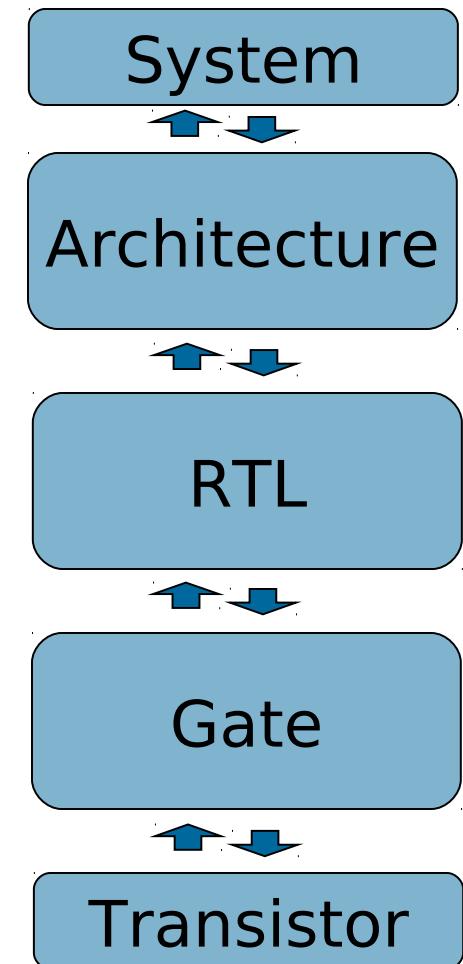


Soure: A. Garcia Ortiz

IC Design Flow



- Because of complexity, IC design must be done following a divide and conquer approach
- At each step, part of the information is “abstracted”
- Depending on the application, there are different design flows and abstraction levels
 - Architecture vs. Behavioral level
 - Hardware-Software co-design

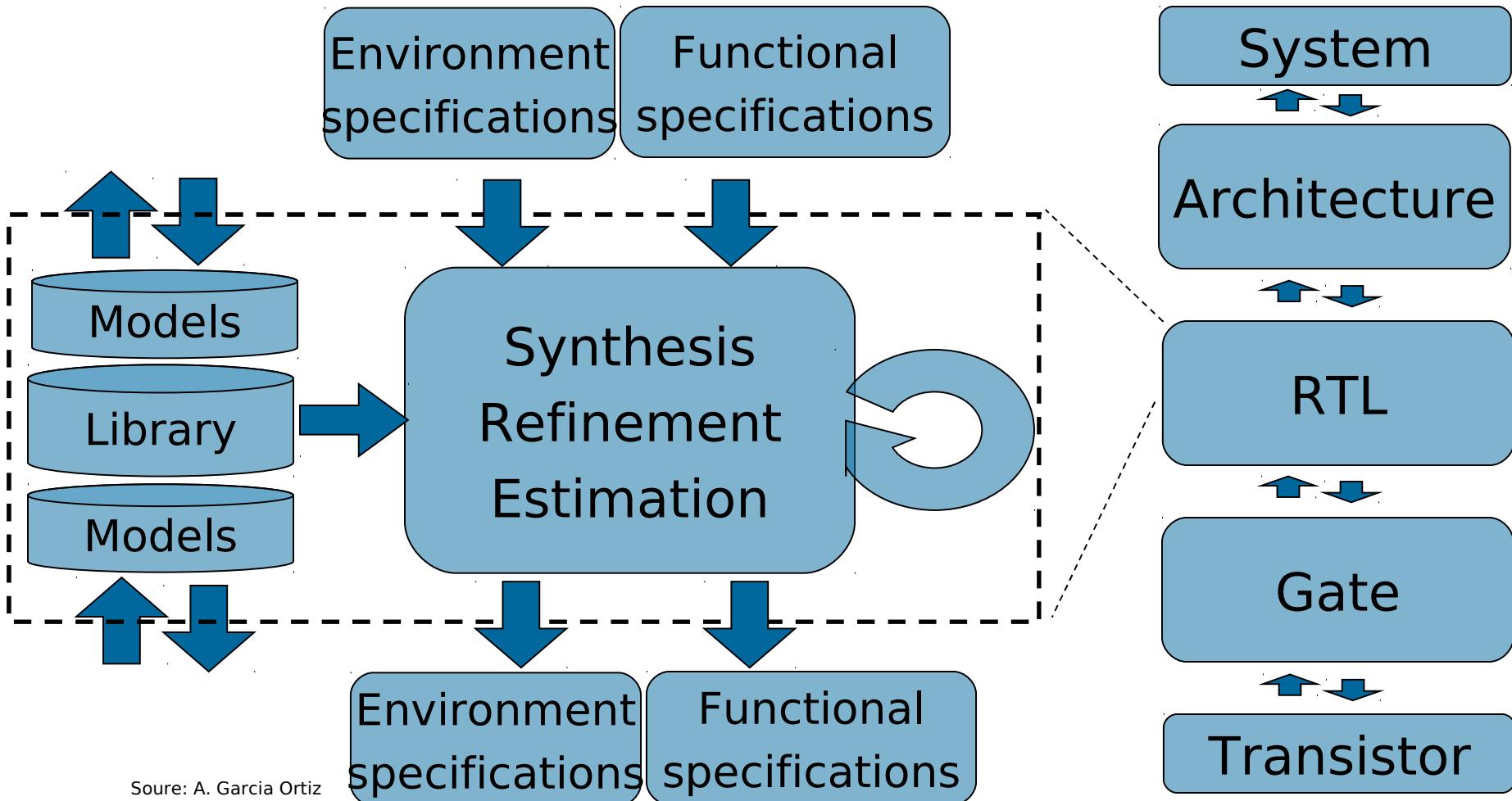


Soure: A. Garcia Ortiz

IC Design Flow (details)

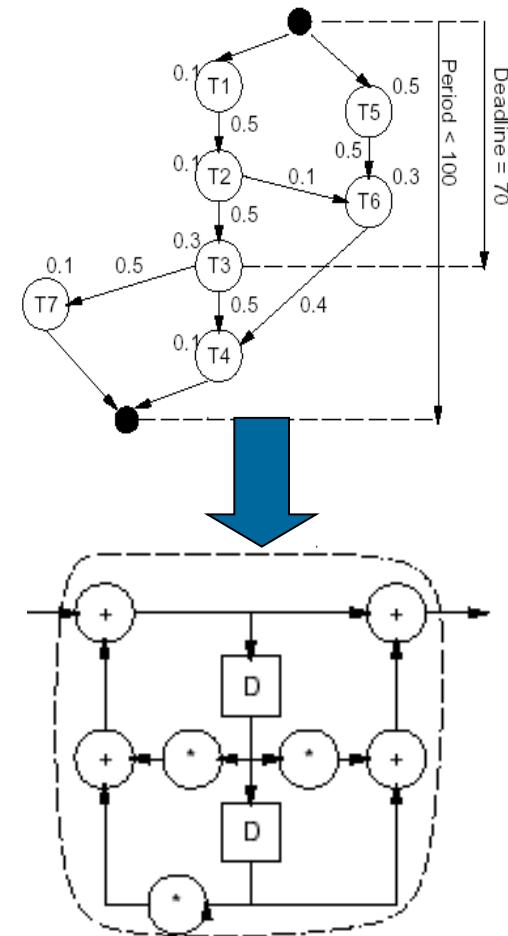
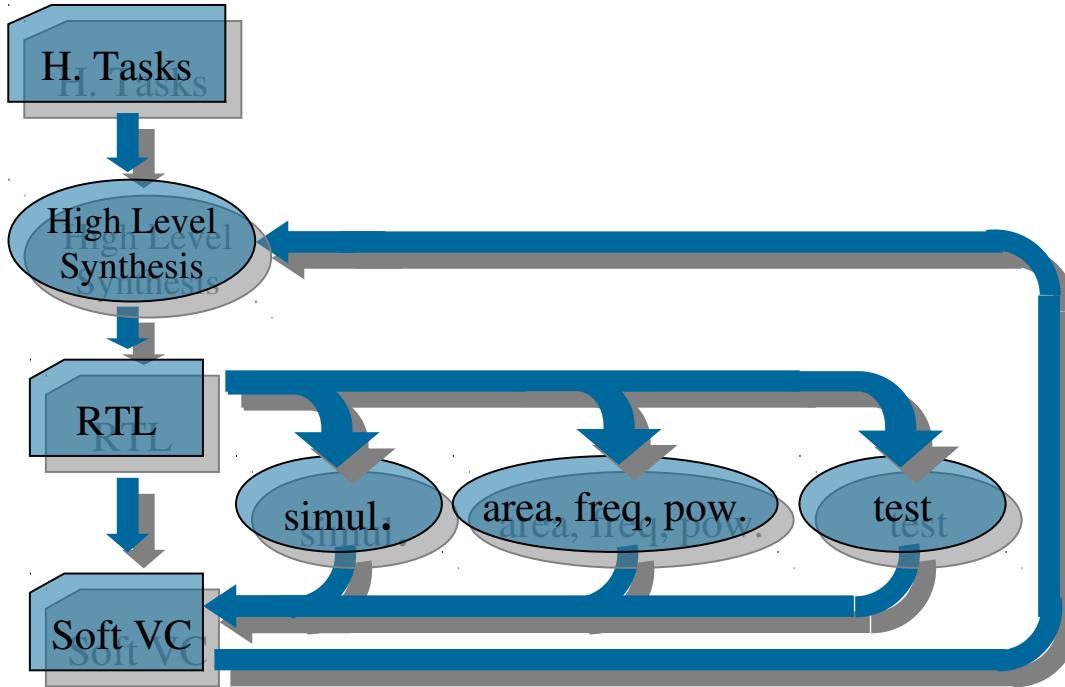


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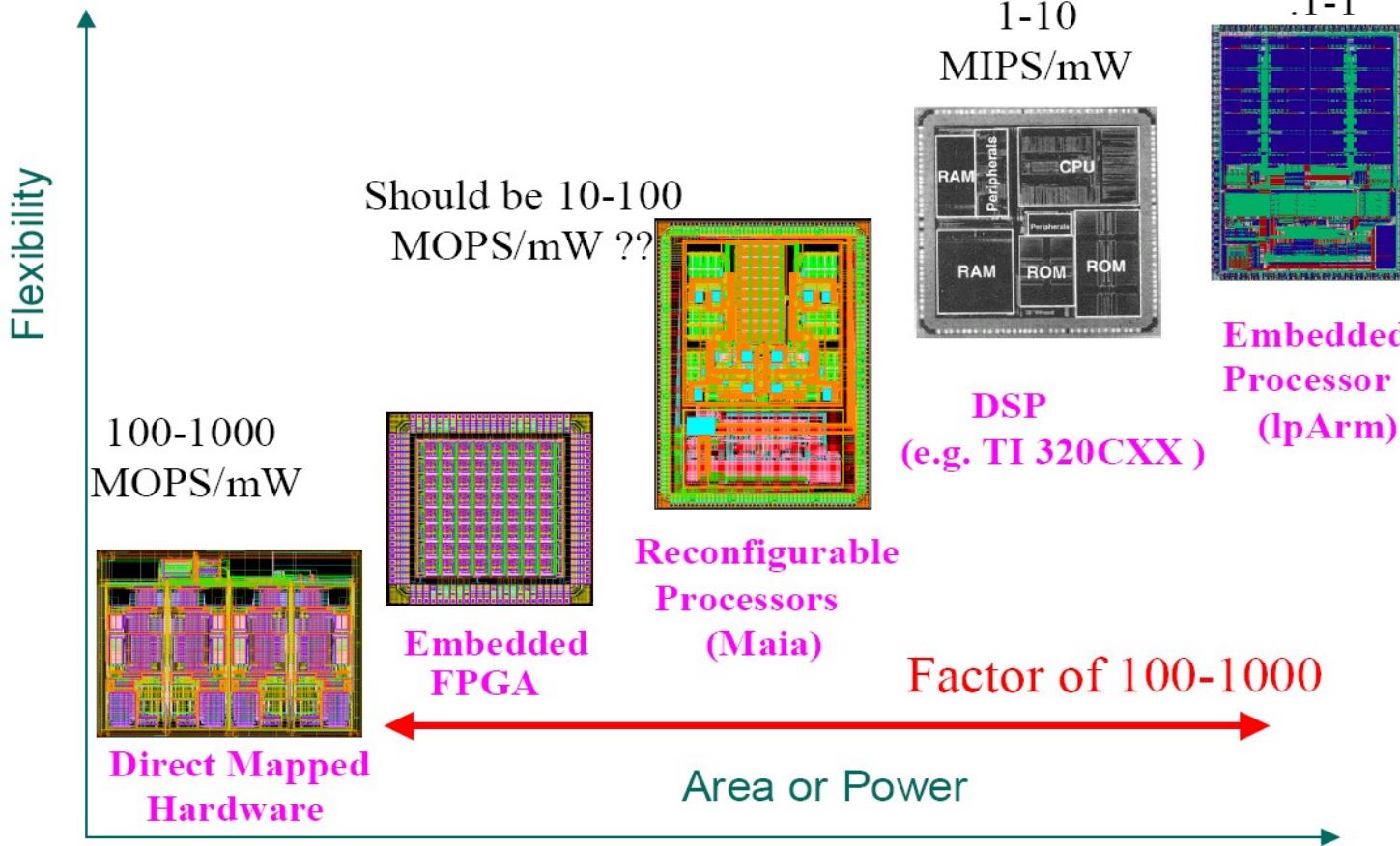


Soure: A. Garcia Ortiz

High Level Synthesis

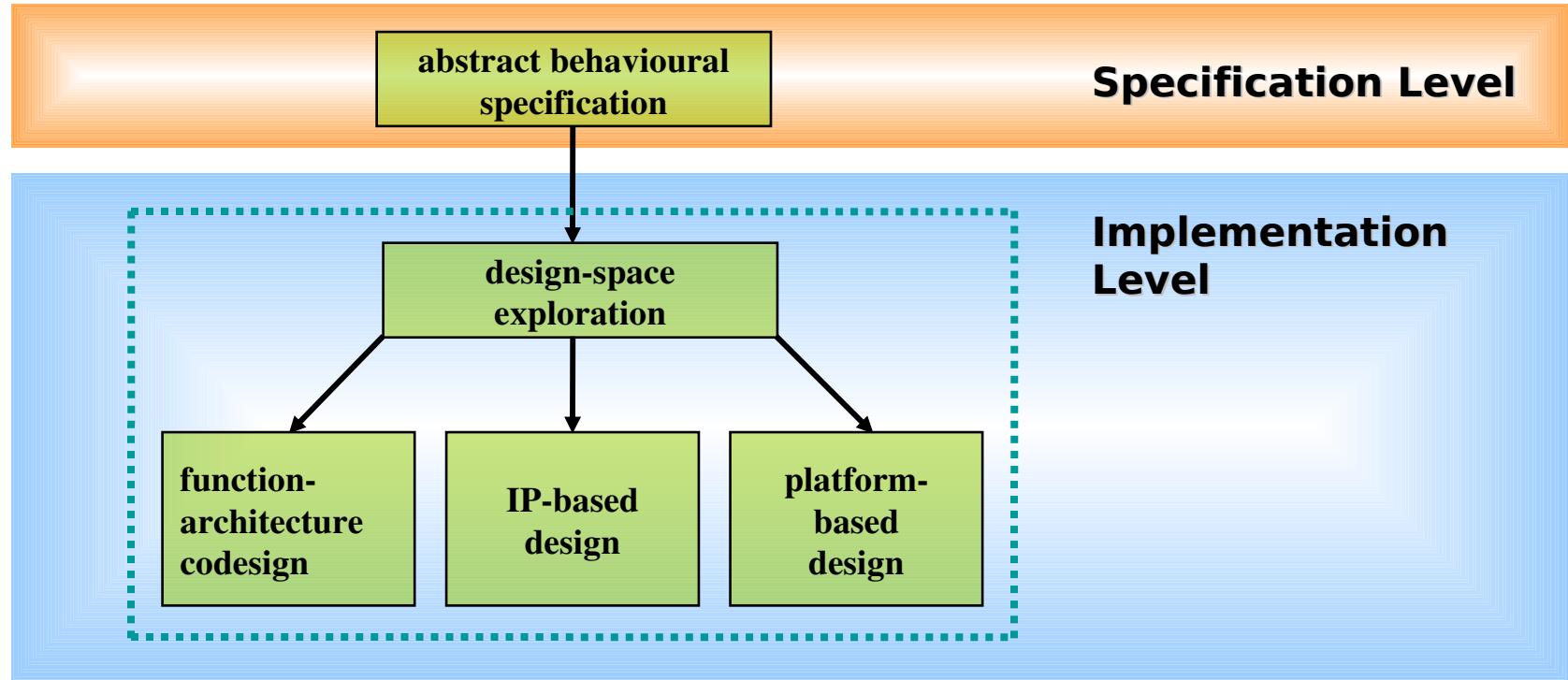


Architecture Alternatives



Source: Berkeley Wireless Research Center

System-Level Design Methodologies



- Important requirements for a methodology:
- **Re-use** (IP, platform)
- **Communication**
- **Testability**
- Reuse requirements:
 - Platform/architecture definitions
 - IP characterization/customisation for easy re-use

SoC Design Challenges



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Silicon Complexity

Complexity Large number of interacting devices and interconnects

System Complexity

- Embedded SW as a key design problem
- Integration of various design styles (analog, RF, electro-optical)
- Integrated passive elements

Design Complexity

Complexity Specification and estimation of multi-domain systems

Verification Complexity

- Formal methods for system-level verification
- Early high-level timing verification

Testability

Complexity Test of core-based designs of multiple sources

Outline



- Status of the electronics industry
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 - Smart Grids
 - Healthcare
 - Adaptronics
- Making the world “smart”, reliable and energy-efficient Wireless sensor networks

Humanity's Top 10 Problems



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1. Energy

2. Water

3. Food

4. Environment

5. Poverty

6. Violence, Terrorism, War

7. Disease

8. Education

9. Democracy

10. Population

- **Energy** is key to most of the other problems on the list.
- It has to be clean!
 - renewable energy must be harnessed to a greater extent
- It has to be cheap!
 - so that developing countries can afford the state of the art

Source:

R. E. Smalley, The Terawatt Challenge

Humanity's Top 10 Problems



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1. Energy
2. Water
3. Food
4. Environment
5. Poverty
6. Violence, Terrorism, War
7. Disease
8. Education
9. Democracy
10. Population

- The top 3 problems are related!
- Water is required
 - as a power plant coolant
 - for farming
- Energy enables
 - water desalination
 - artificial irrigation
 - fertilizer production
- Water resources are threatened
 - by fossile fuel mining
 - by overfertilization
- The IEEE's magazine *Spectrum* is running a special report „Water vs. Energy“ this month

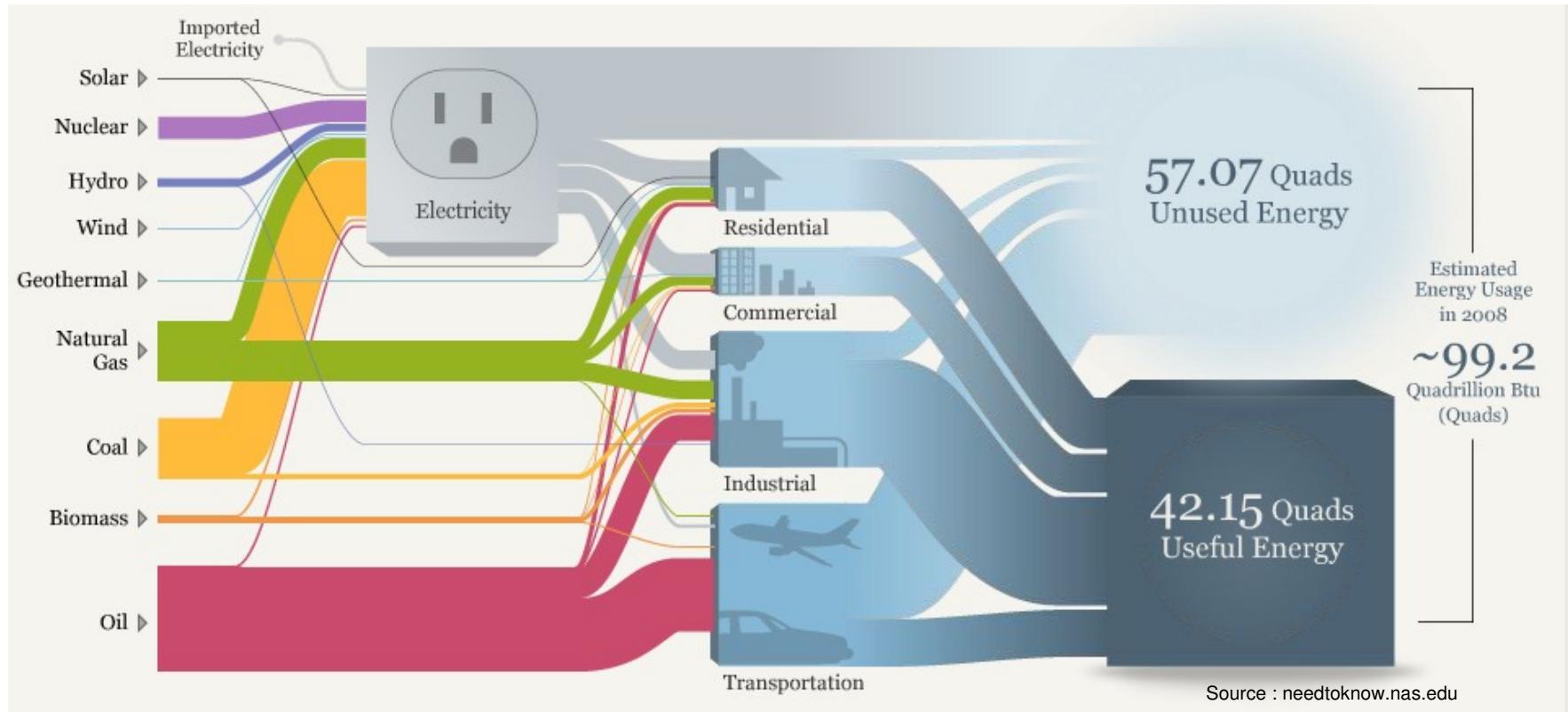
Sources: R. E. Smalley, The Terawatt Challenge /
IEEE Spectrum

State of the U. S. Energy System



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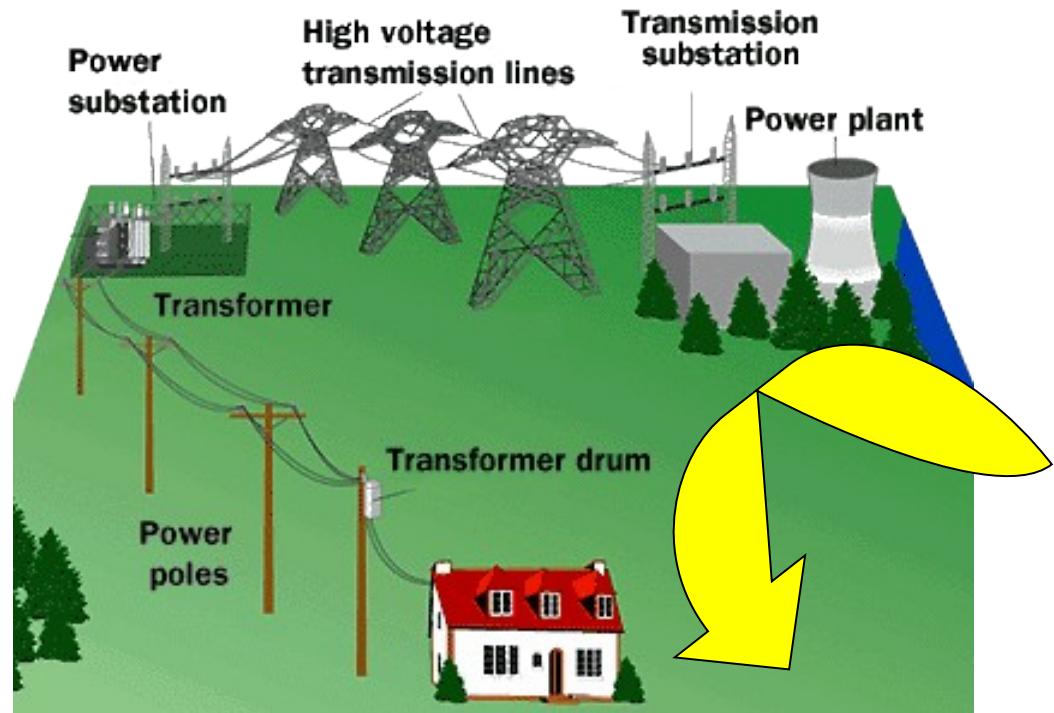
- About the half of the energy created is wasted !
- Needs **optimisation**



Current Power Grid



- “**Top-Down**” approach for load flow
- Power is transmitted from generators to consumers at different voltage levels
- Grid is centrally controlled
- Grid is optimized for regional power adequacy



Source : bordalierinstitute.com

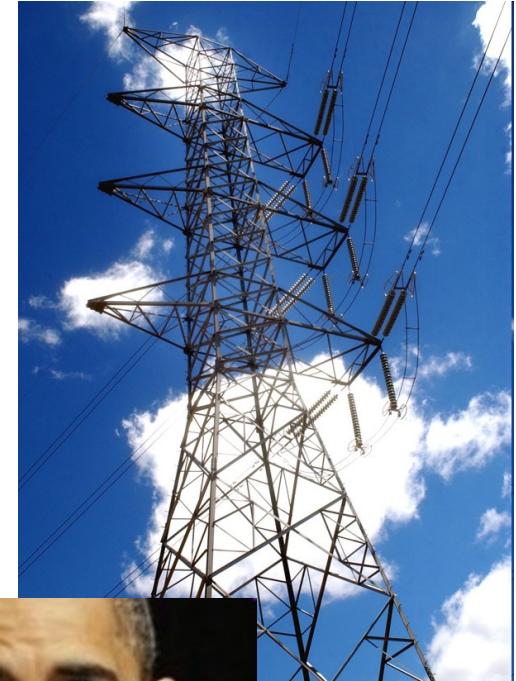
- “As far as the communication with the consumers is concerned, the energy industry is effectively the last industrial dinosaur”
Dierk Paskert, E.ON board of directors, in a newspaper interview published on June 7, 2010

Smart Grids



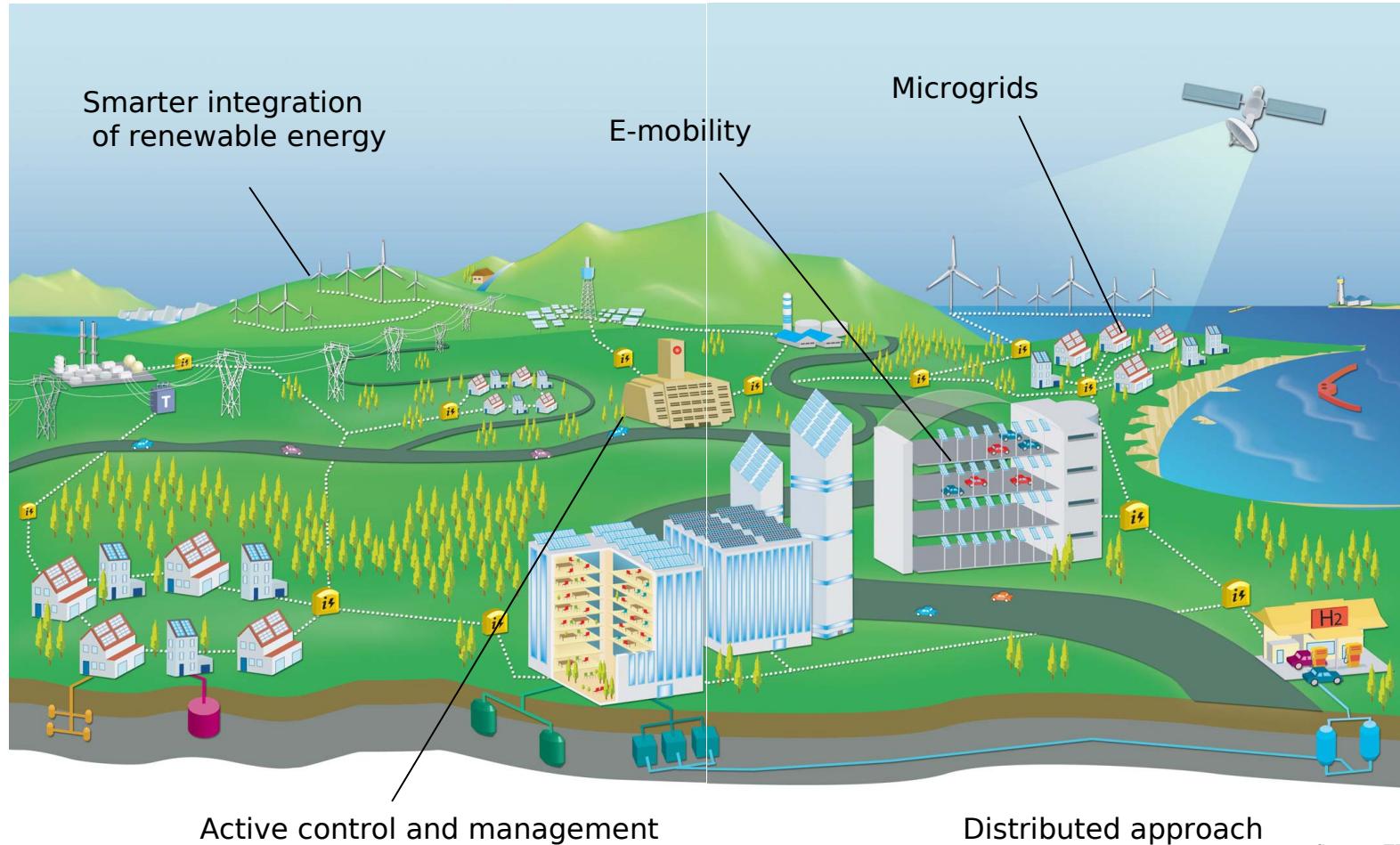
- New conception of electricity distribution
- Better usage of renewable energy
- Increase **energy efficiency**
- Reduce **costs**
 - e. g. by distributing peak demand more evenly
- B. Obama announced a \$ 3.4 B plan to update the U.S. grid

Source : eftrends.com



Source : wn.com

Smart Grids

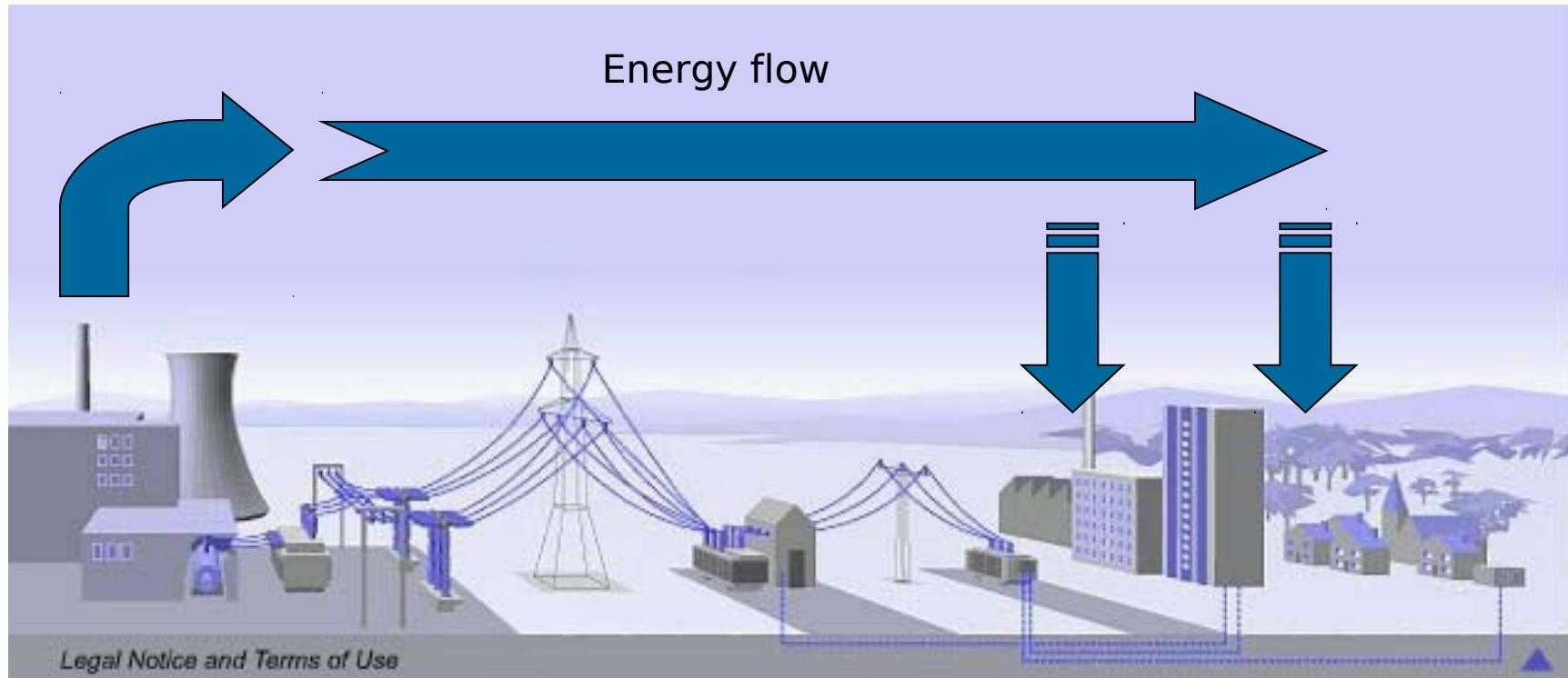


Source : EUR 22040

Bi-Directional Distribution



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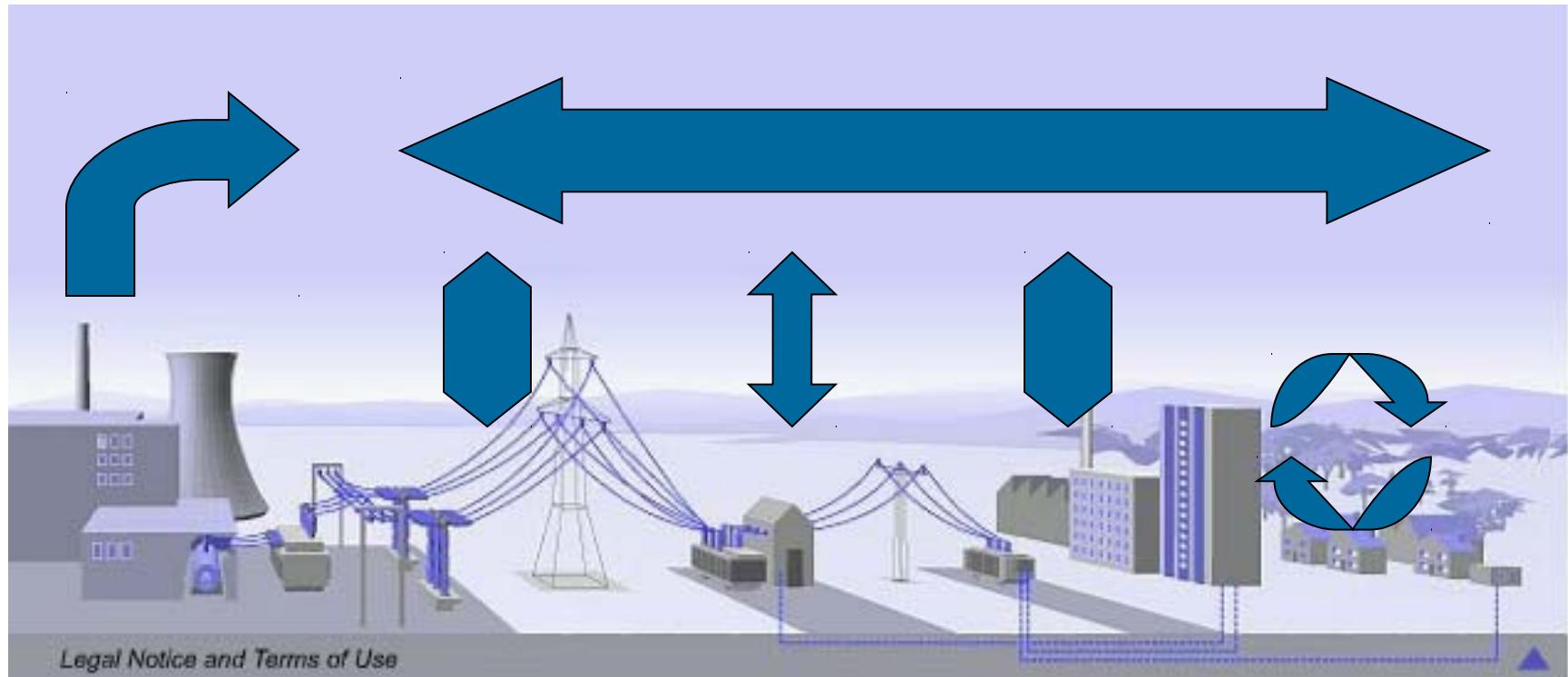


Today

Bi-Directional Distribution



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Tomorrow

Enabling Technologies



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▪ Integrated communication

- Power line and wireless communication
- Plug-and-Play
- Open source / Secure
- Dynamic exchange of energy and information
- Real-time and secure
- Support for huge amount of data

▪ Sensors and measurements

- Estimation of consumption
- Health monitoring and Grid maintenance
- Congestion avoidance

Enabling Technologies



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▪ Dynamic regulation and optimization

- Active distribution networks
- Consumer participation
- Distributed management

▪ New grid technologies

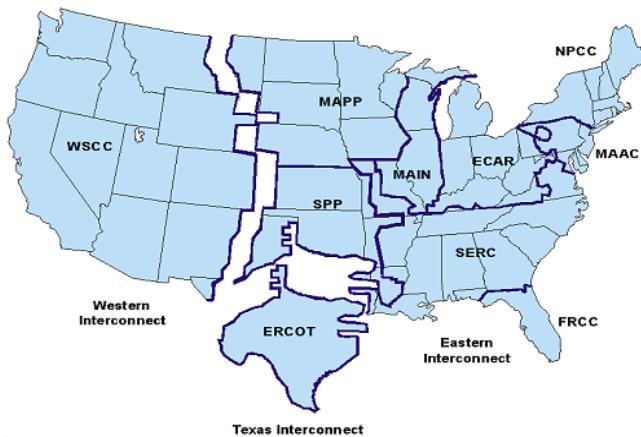
- High Voltage DC Transmission
- Superconductivity
- Power electronics for improved quality of supply
- Stationary energy storage devices

Synergies between Electronic Design Automation and Smart Grids



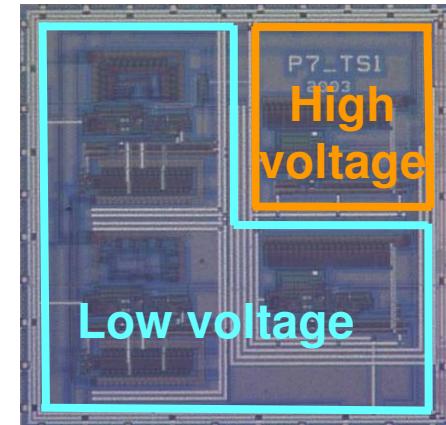
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US Power Distribution System

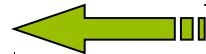


9 629 091 km²

IC Power Distribution Grid



Factor 1.5×10^8



6 cm²

- *A priori* completely different
- But similar problem formulations

Synergies between Electronic Design Automation and Smart Grids



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Smart Grid:

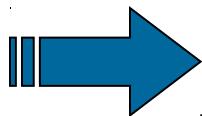
- System Management
- Simulation
- Modeling
- Optimization
- Fault Detection
- Security

- Analysis
- Design
- Management

Electronic Design Automation:

Widely-employed in electronic system design

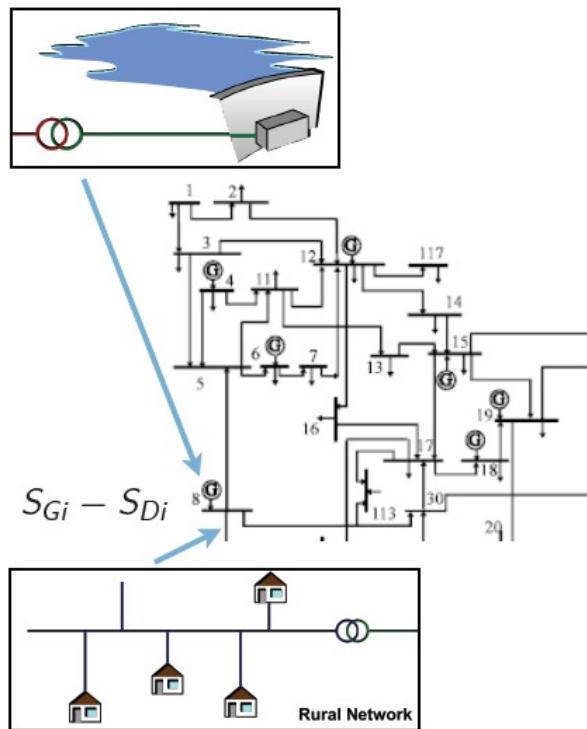
Find new application in the electronic system design



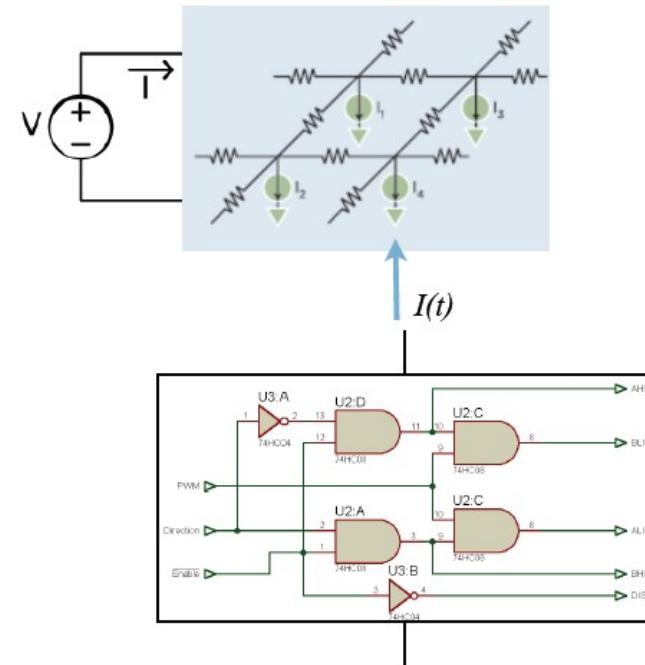
Grid Abstraction



- Electric Grid: Power Sources



- Chip Grid: Current Sources

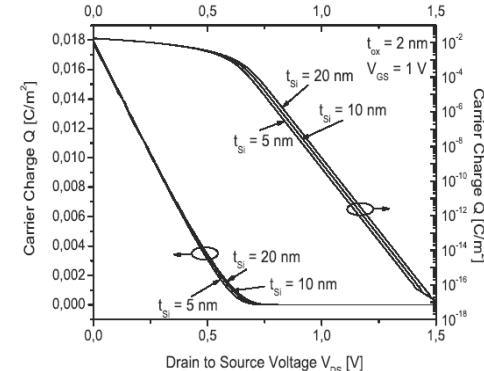
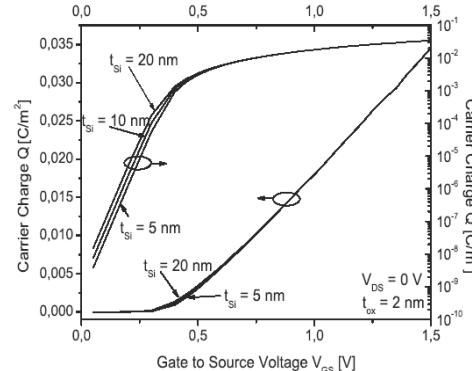
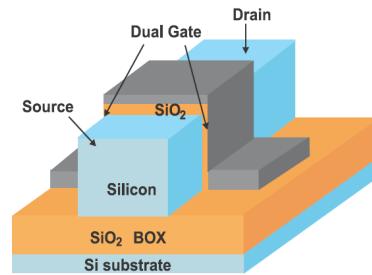


Source: P. Feldmann, DAC2010

Modeling, Simulation, and Optimisation

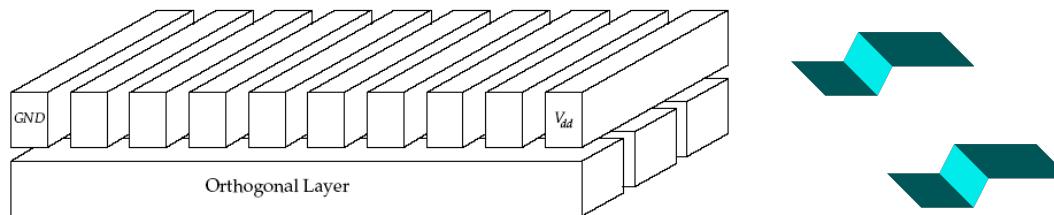


- Modeling in Electronic Design Automation:
 - Device Models (e.g. Double-Gate SOI MOSFET):



- Gate-Level:
 - Static Timing Analysis (STA), Statistical STA
 - Power Estimation using estimated switching activity and interconnect models

Source : Oana Cobianu



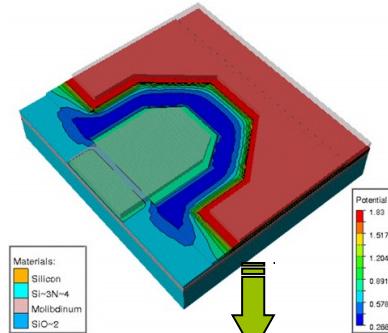
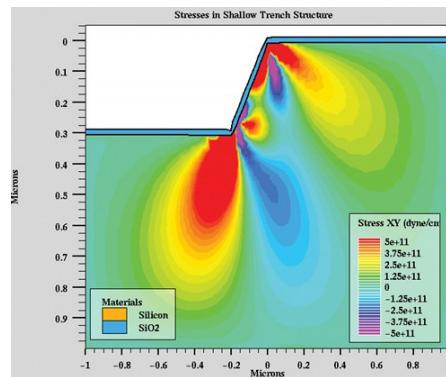
$$E = \frac{V_{dd}^2}{2} (C_s t_s + 2C_c t_c)$$

Source : T. Murgan

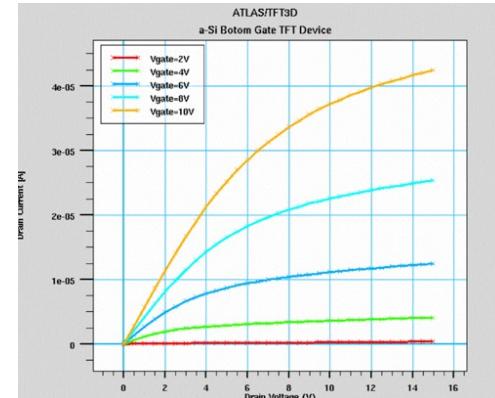
Modeling, Simulation, and Optimisation



- Simulation in Electronic Design Automation:
 - Device-Level (e.g. Silvaco Atlas/TFT3D, SSuprem etc.):



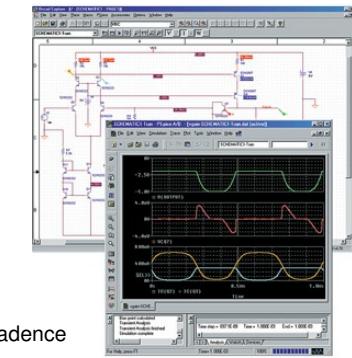
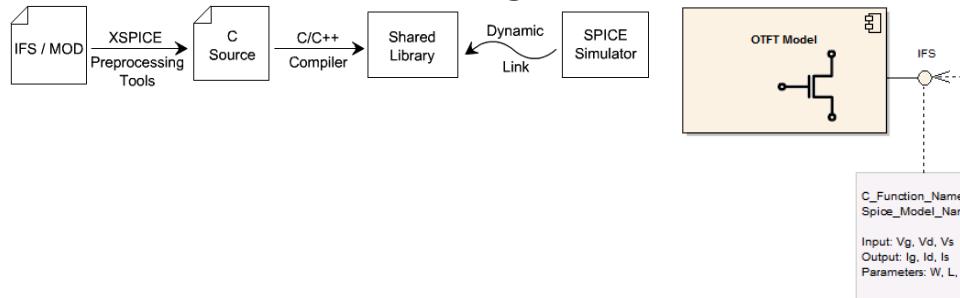
also for printed/organic transistors



Source : www.silvaco.com

- Circuit-Level Simulations (SPICE, Spectre/Cadence etc.):

- Embedding of custom models

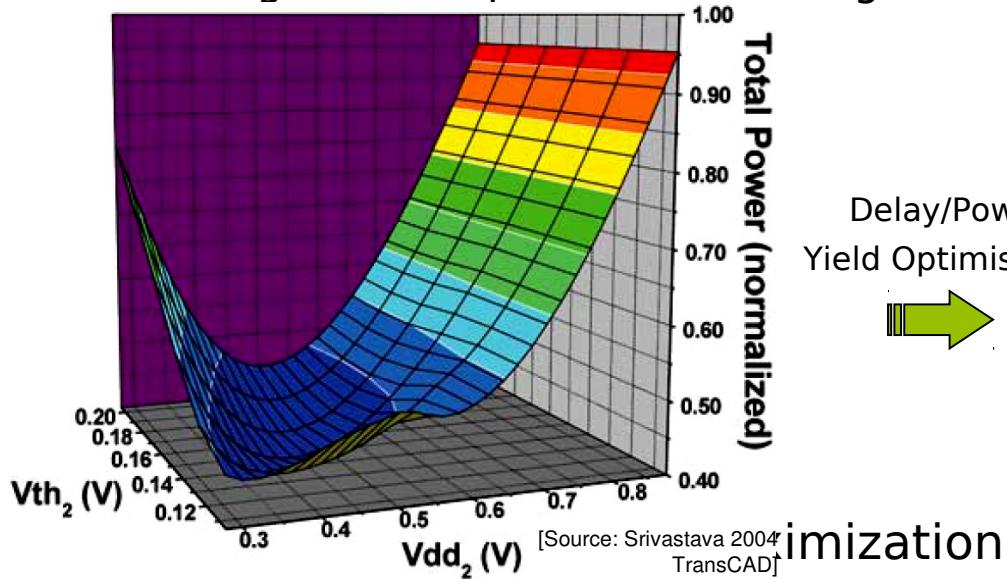


Source : Cadence

Modeling, Simulation, and Optimisation



- Optimisation in Electronic Design Automation:
 - e. g. Power Optimisation through Voltage Scaling and Body Biasing

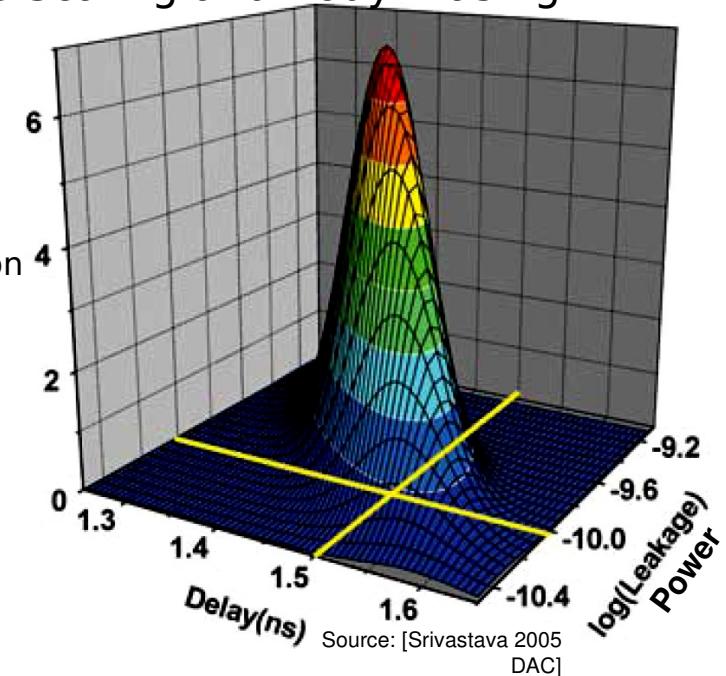


Delay/Power
Yield Optimisation

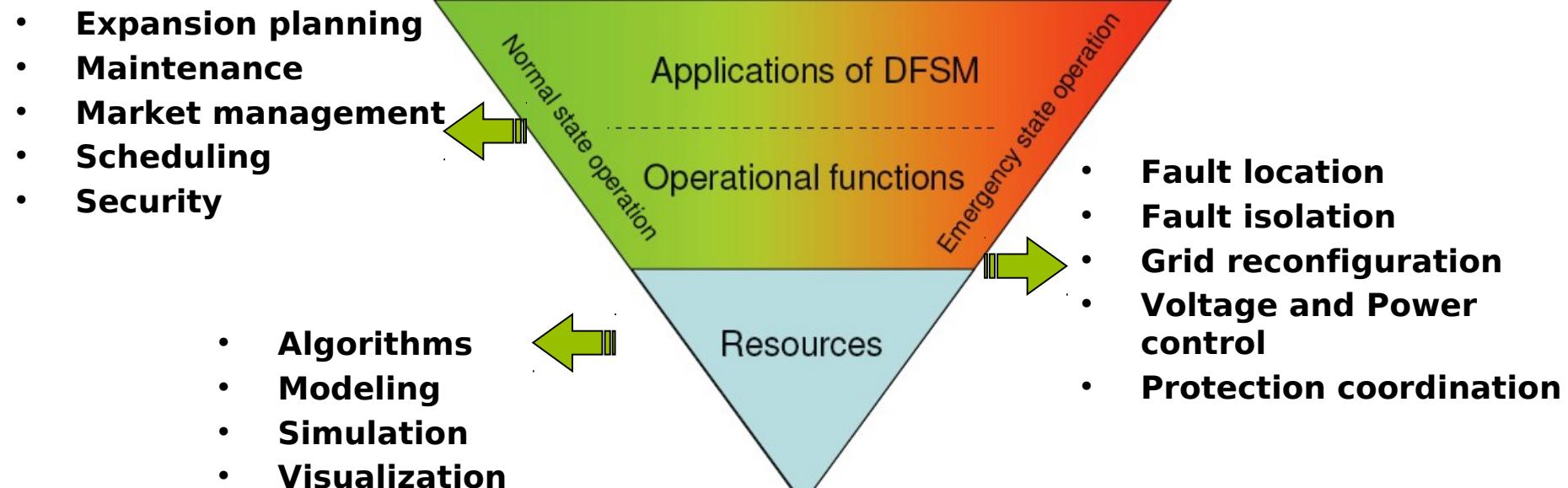


Optimization

- Statistical methods
- Combinatorial optimisation algorithms
- Cost functions: performance, power, size



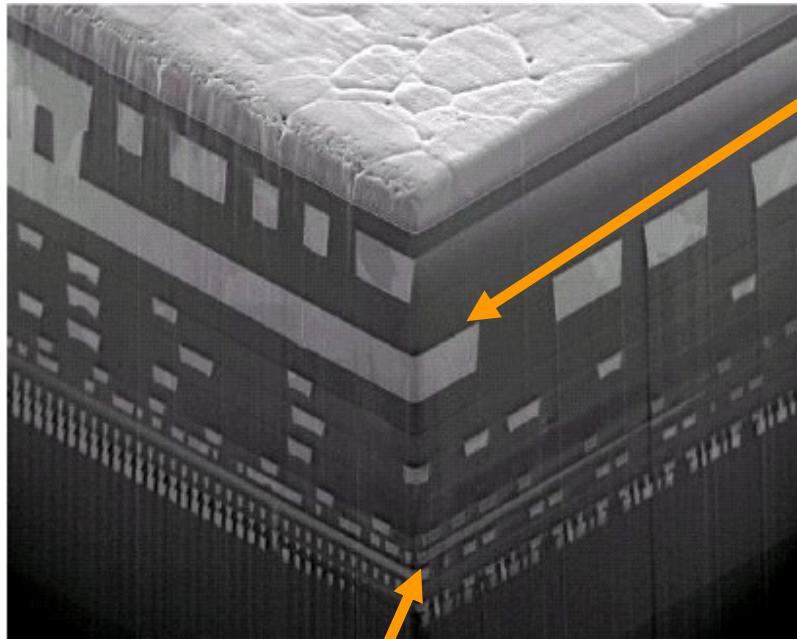
Simulation Needs



Example: 90 nm



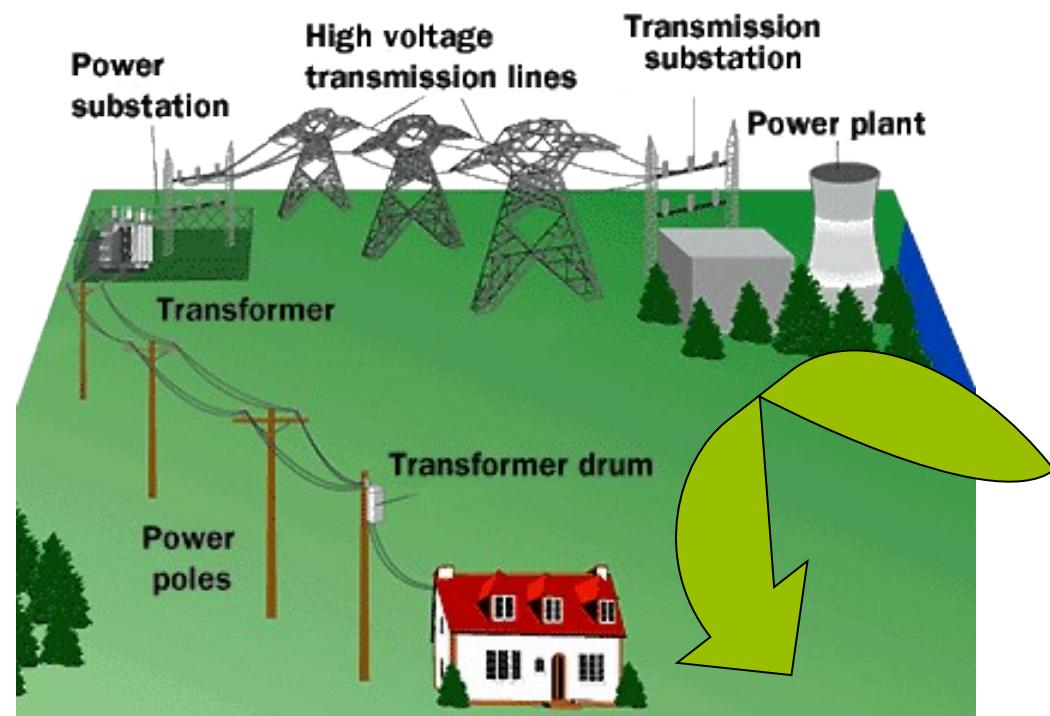
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Local
interconnects

Global
interconnects

Source : IBM



Source : bordalierinstitute.com

Outline



- Status of the electronics industry
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- Strategic research directions
 - Smart Grids
 - **Healthcare**
 - Adaptronics
- Making the world “smart”, reliable and energy-efficient Wireless sensor networks

Wearable Computing



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- In developed countries, healthcare systems will change radically, driven by cost and quality issue.
- New micro and nano technologies coupled to low-power computing, wireless communication and information processing enabled **pervasive, mobile** biomedical measurements and health monitoring.
- Smart miniaturized sensors, data processing and communication devices will be embedded in our daily outfit :



Wearable Computing



Source : Imec

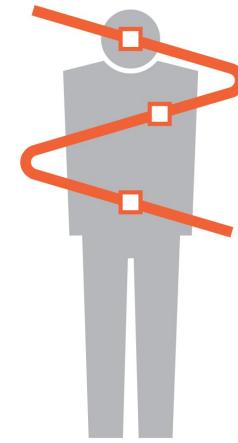
Body Area Networks



- Body area networks consists of intercommunicating sensors monitoring vital health signs and body movements
- Last generation of low power, wireless sensor nodes have enough computation capabilities to analyse data locally and alert patient or doctors immediately.
- Very long lifetime can be achieved for these devices with recent improvements in **energy harvesting** techniques.
- Energy scavenged from body heat and moves is sufficient to supply body area networks for several months !



Fhg.de

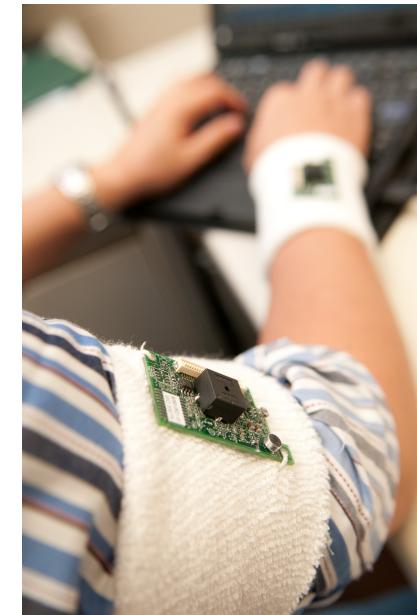
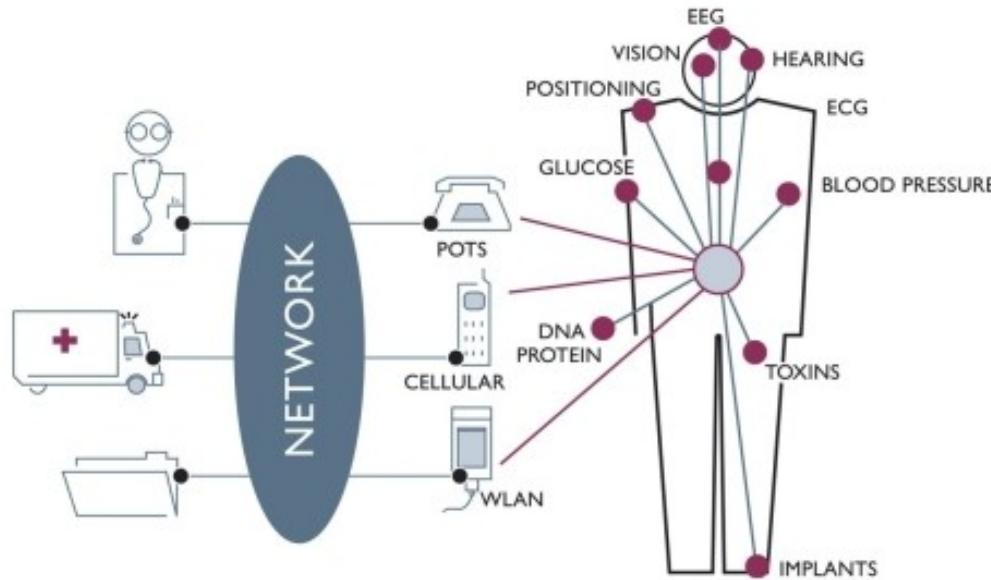


Ethz.ch

Internet of Things and Healthcare



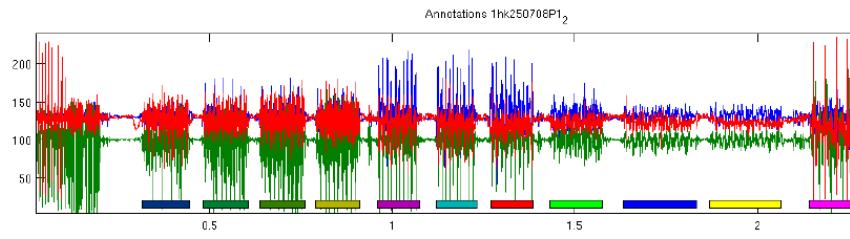
- Sensors are able to communicate with complex embedded computing systems, our cell phones or personal computers
- Our health state is transmitted **in real time** through the Internet to doctors / emergency medical services / or database allowing direct intervention in case of problem.



Actigraphy



- Actigraphy is a method of monitoring human rest/activity cycles.
- Movements of the patient are recorded and analysed
- Identify pathologies of bipolar disorder / sleep troubles
- Enabled via small, low power, wireless sensing systems



Porcupine project

imec.be

Internet of Things and Healthcare



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- Information circulates through every day object such as key rings, USB keys or entertainment devices
- Transparency and wearability



Glucose sensor :
Data is stored in the USB stick and can be transferred to a cell phone

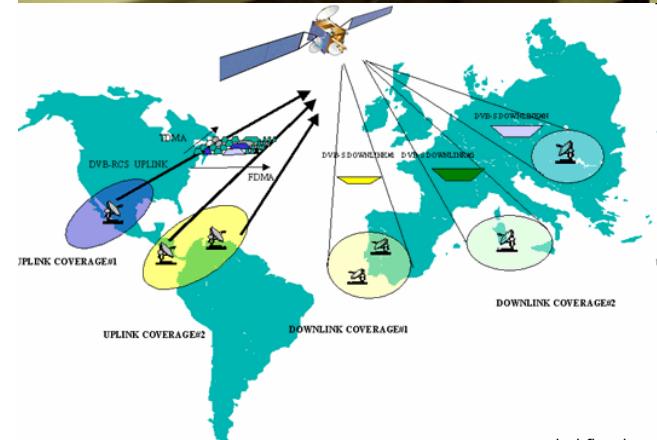


Vital Key ring :
Store all vital signs of a patient for rapid diagnosis and emergency procedures

Telemedicine



- Thanks to recent improvements in communication infrastructures, advanced medicine is yet available remotely to distant and hardly accessible regions
- New microelectronic technologies enables **low-cost, portable** and **reliable** health diagnosis instrumentation
- Diagnosis stations and medical equipment can be accessed by isolated patients who can directly communicate with doctors located anywhere in the world !



Outline



- Status of the electronics industry
- Research overview @ MES
- System Design
- Strategic research directions
 - Smart Grids
 - Healthcare
 - **Adaptronics**
- Making the world “smart”, reliable and energy-efficient Wireless sensor networks

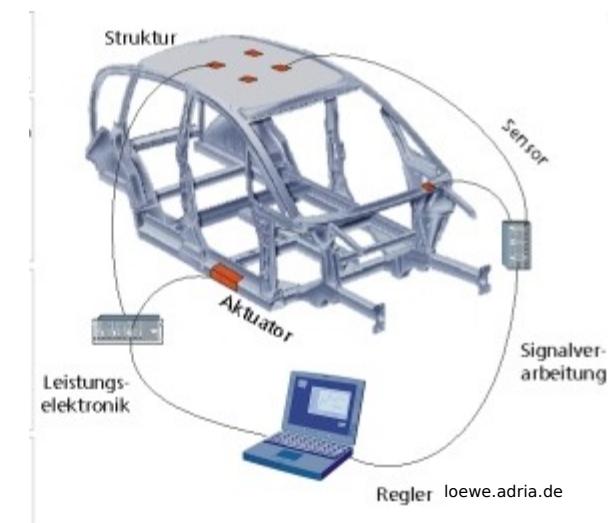
Adaptronics



- **Adaptronics** is an interdisciplinary technology bringing together microelectronics, mechanical engineering, computer science and control engineering
- Development of smart adaptive structures and material
- Mechanical systems and actuators, controlled by central or distributed controllers, react in real time to changing environmental conditions detected by specific sensors



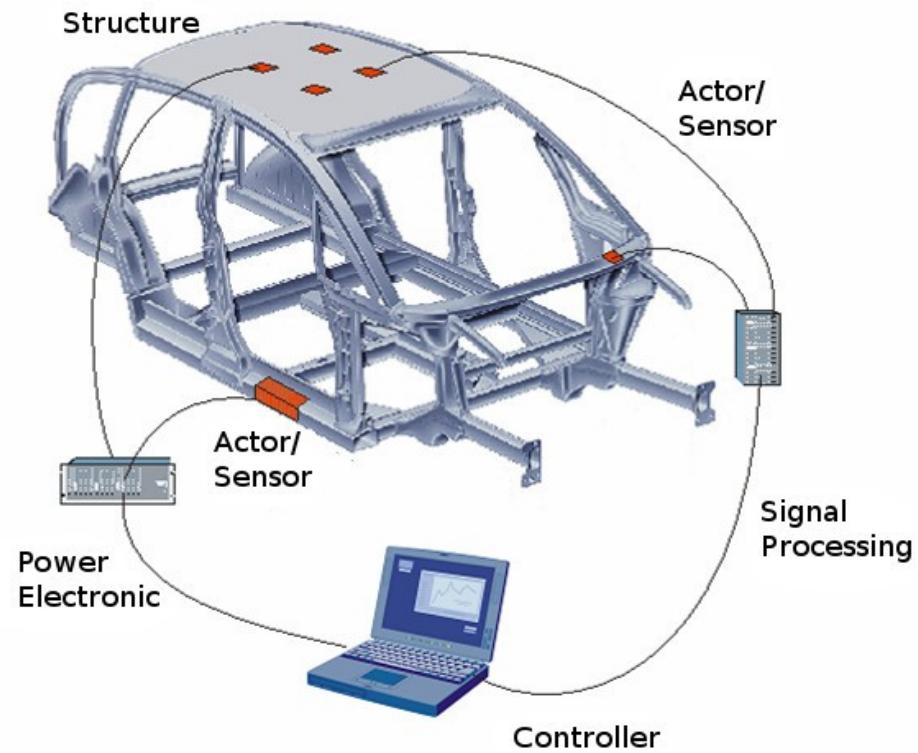
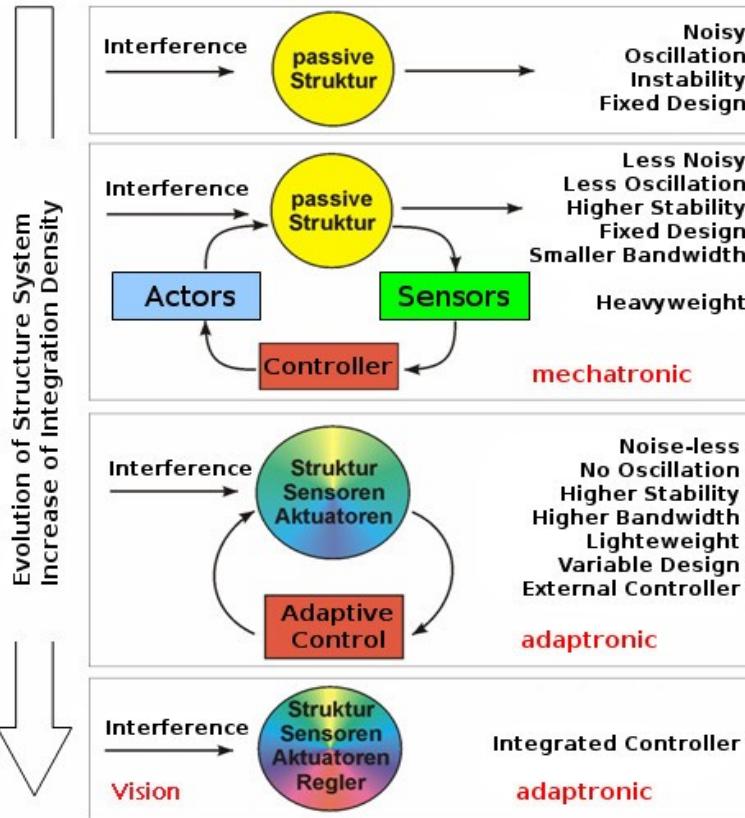
Intelligent systems



Adaptronics



- Evolution of complex system design



Motivation



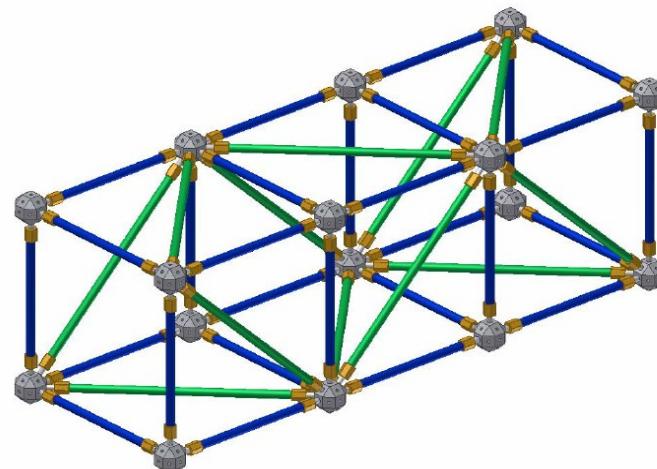
- Collaboration with many technology experts: Chemicals, Materials, Printing, Sensors, Mechatronic, Control Systems, System Design, Distributed Processing, etc.
- Early integration of the concepts of controller to the conceptual design is very crucial
- Boundary conditions are derived from the concepts of the controller for adjacent Technologies (Sensors, Actors, Electronics, System Reliability, etc.)

Adaptive Bearing Networks

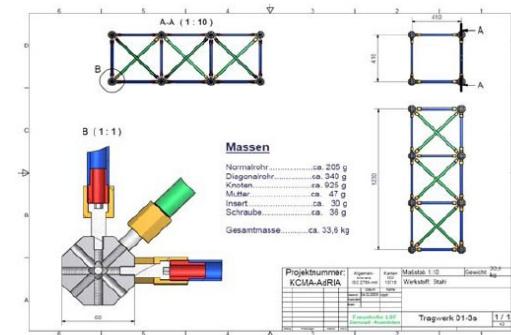


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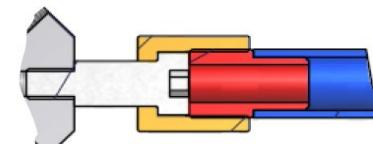
- Modelling
- Vibration Control
- High Quantity
- Distributed & Centralized Controls



3D Illustration



Construction Scheme



Connecting Element

Conclusions



- New technological areas where Electronics have a major role to play
 - Smart Grids
 - Healthcare
 - Adaptronics
- Enabled by new generation of embedded systems
 - Smaller
 - Lower power consumption

Outline



- Status of the electronics industry
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- System Design
- Strategic research directions
 - Smart Grids
 - Healthcare
 - Adaptronics
- Making the world “smart”, reliable and energy-efficient
Wireless sensor networks

Intelligent Systems



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- All models defining intelligent systems are inadequate.
But some models are useful.
- Intelligent behavior =Reasoning and Optimization through Experience supported by Communication

(Board of Scientific Affairs of the American Psychological Association, 1995)

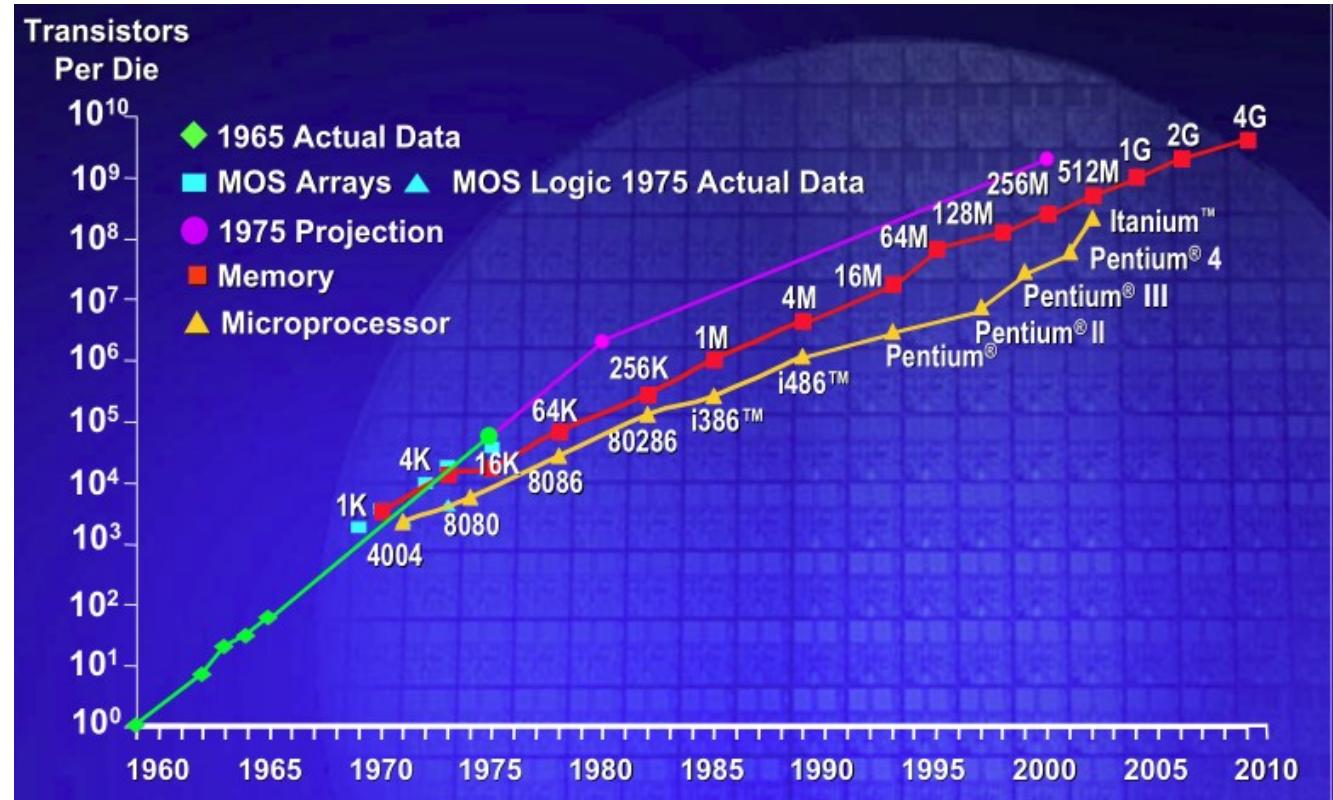
- This type of optimization means adaptation to new situations
- An intelligent system may contain *sensors*, *actuators*, a *cognitive unit* and *intra-system communication means*
- This description also fits embedded computers!

Source: Prof. Saman Halgamuge, Univ. of Melbourne, Australia

Where does it come from



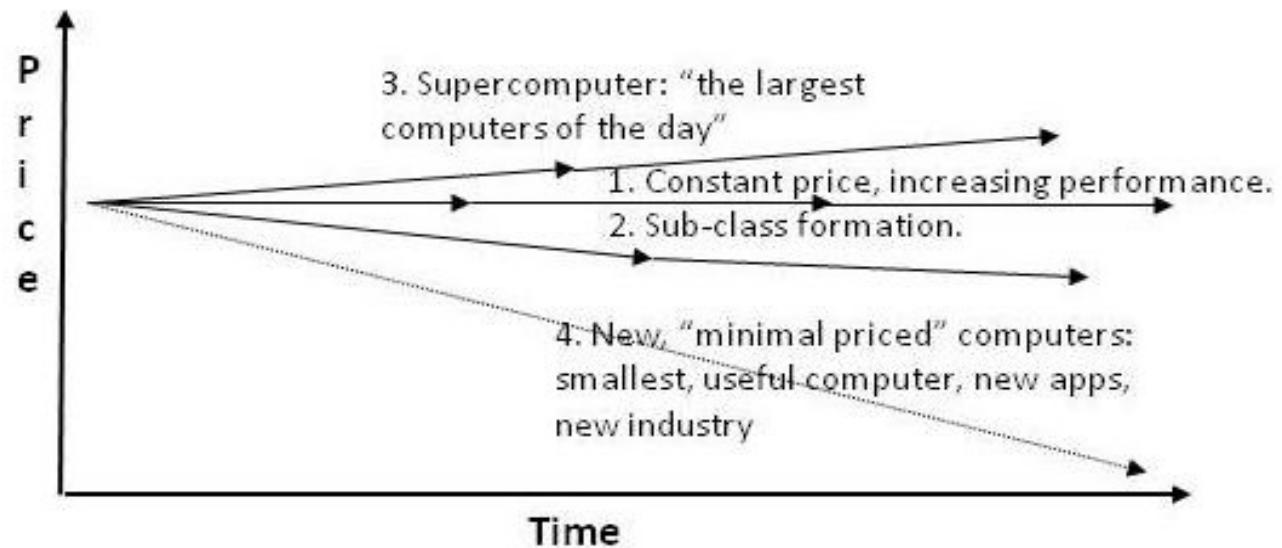
- Moore's Law (1965)



Where does it come from



- Moore's Law
(1965)
- Bell's Law
(1972)



Where does it come from



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- Moore's Law (1965)

- Bell's Law (1972)

- Mark Weiser,
Ubiquitous Computing
(1991)

▪ The Computer for the 21st Century

- "Specialized elements of HW and SW, connected by wires, radio waves and infrared, will be so ubiquitous that no one will notice their presence."



Source : parc.com

- "The most profound technologies are those that disappear. They weave themselves into the fabric of everyday life until they are indistinguishable from it."

Scientific American, September 1991

▪ The World is not a Desktop

- A new way of thinking is needed, that takes into account the human world and allows the computational resources to vanish into the background

Where does it come from



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- Moore's Law (1965)
- Bell's Law (1972)
- Mark Weiser, *Ubiquitous Computing* (1991)
- Smart dust (2001)

▪ The Computer for the 21st Century

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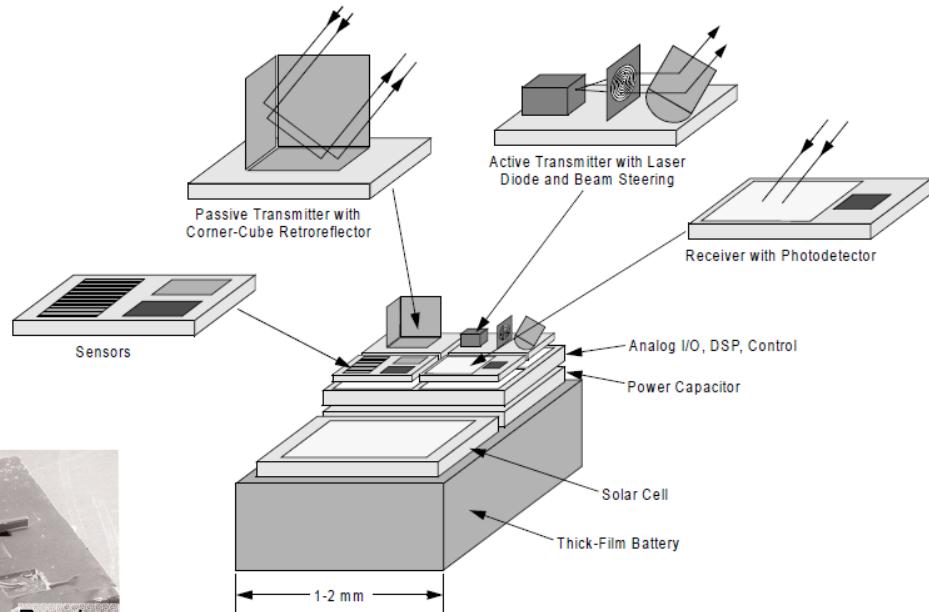
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In Dust We Trust

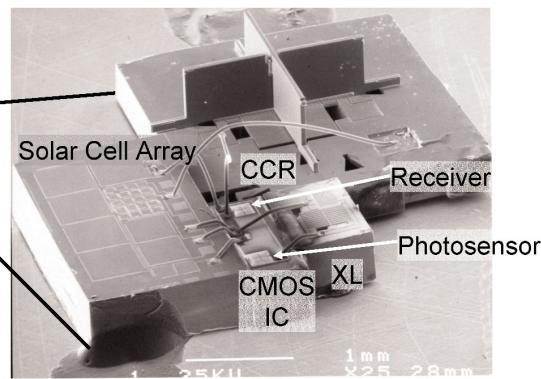


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- The Smart Dust (2001) in reality:
 - Based on optical link
 - Fit in a few mm³
 - Powered by a solar cell



Source : Kahn & al, MobiCOM99

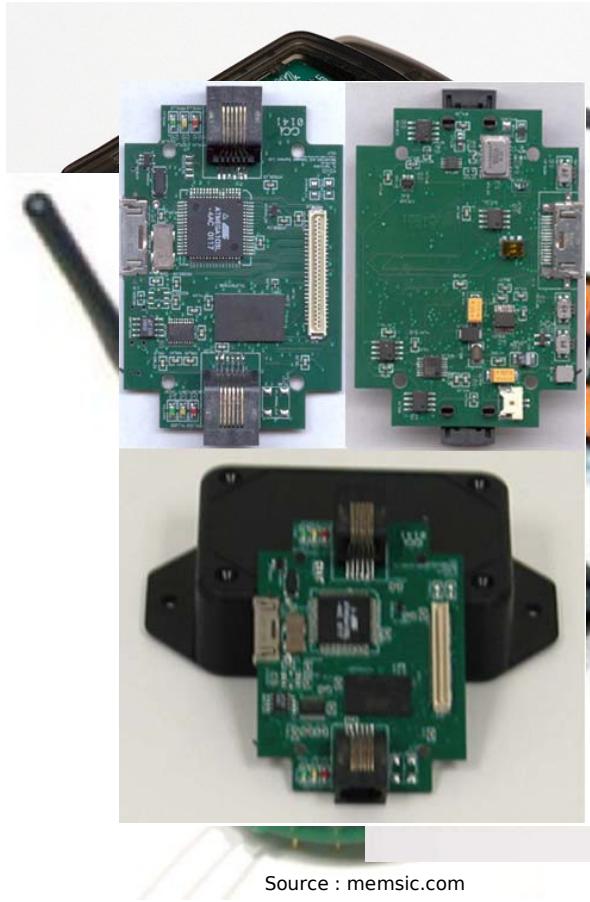


Source : Warneke & al., ISSCC04

The Mote : Meet the Family



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Source : memsic.com



& al, IPSN05

Main Design Challenges



- Power consumption
 - Availability of the network as long as possible
 - Low power Hardware
- Computational capabilities
 - Limited microcontrollers
 - Small memory
- Communication protocols
 - Limited range
 - Limited bandwidth



Energy-Efficiency

Smart sensing



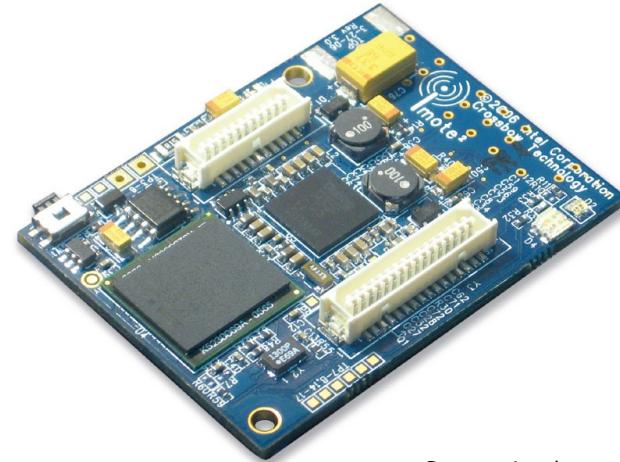
- In Smart Sensor networks, functionality of the mote is not limited to simple sensing and routing
- The Sensor node is capable of analysing the data and taking decisions on itself according to the results
- Dealing with more complex data
- Example : Intruder Detection
 - Detect Real Intruders / not a cat
- Requires higher computational capabilities...

Next generation



- IMote2
 - Developed by Intel
 - Based on a DSP coprocessor running at more than 100 Mhz (!)
 - Thanks to DVFS, power consumption is adapted
 - Still power hungry for networking tasks

- FPGA
 - Our's !
 - Mapped data processing to FPGA
 - Independent from networking

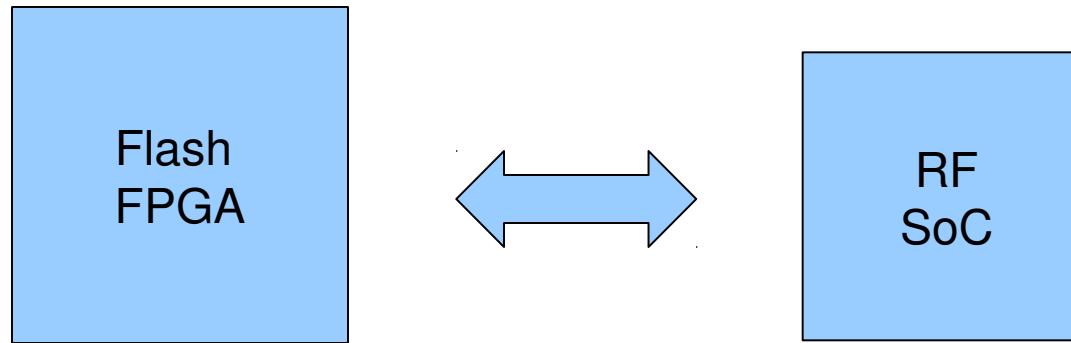


Source: Intel

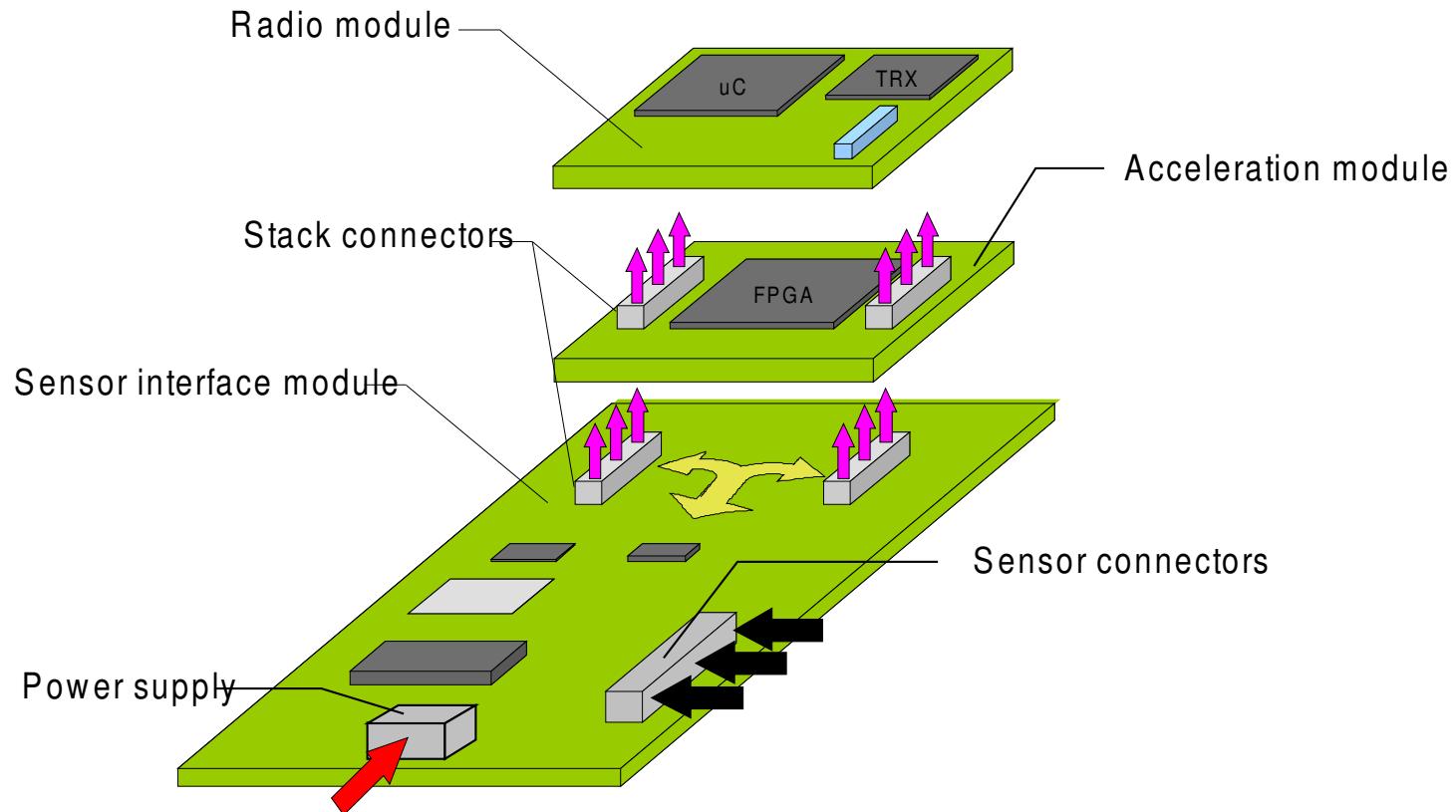
Architecture



- Many I/Os available
- Extendability
- Separate Sensor Data Acquisition / Preprocessing from networking
- Flash FPGA
- Low power consumption and no power up reprogramming required



Overview

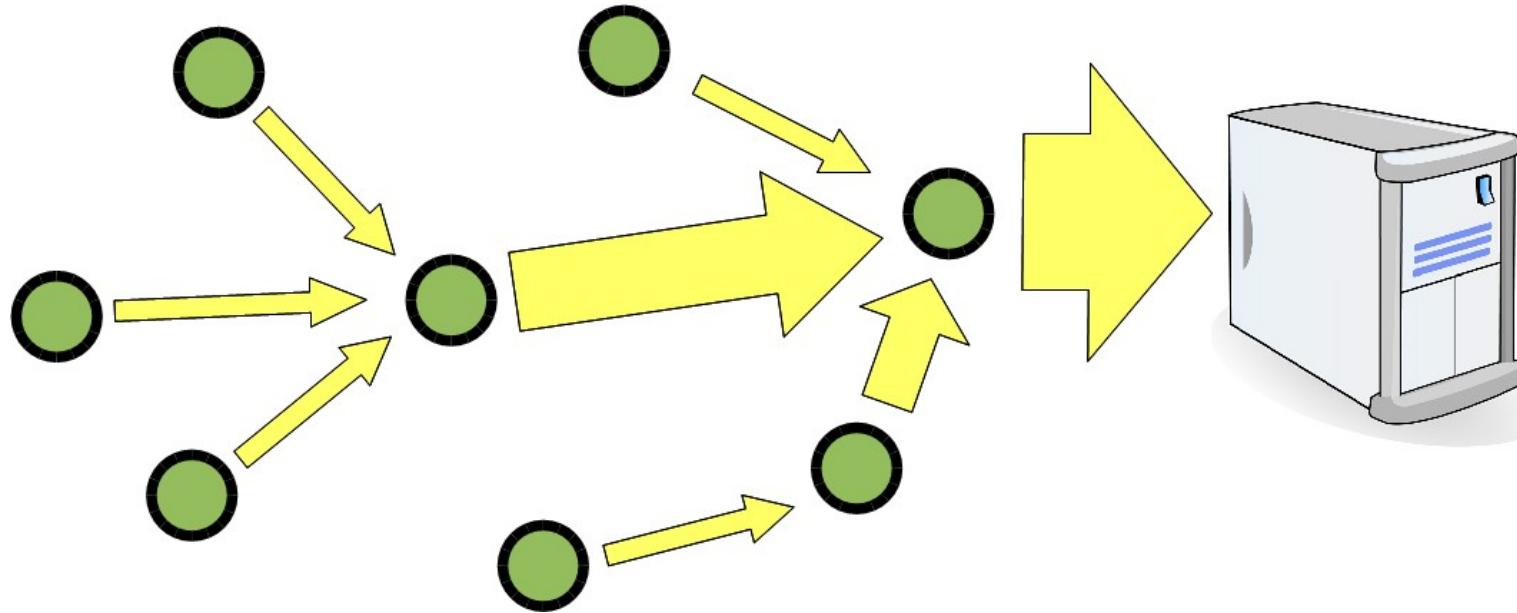


Not only a prototype



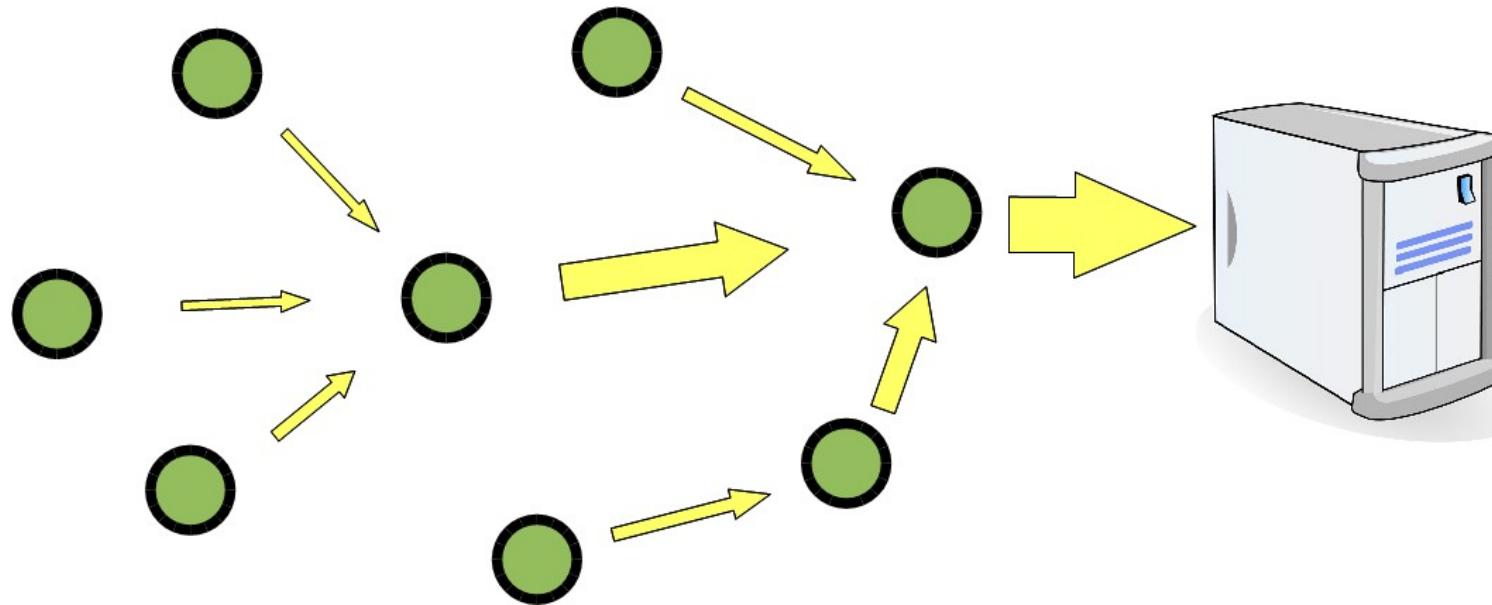
- FPGA is used in our system to increase the flexibility
- Each application requires different sensor interfaces and data processing blocks
- Lower power consumption may be achieved with ASICs but the design costs are much higher
- Today's FPGAs reach near-ASIC power consumption

High Bandwidth Sensing



- Congestion !
- Large Response Time
- Energy unfair routing
- Low power protocols not adapted

Smart Sensing at the Edge



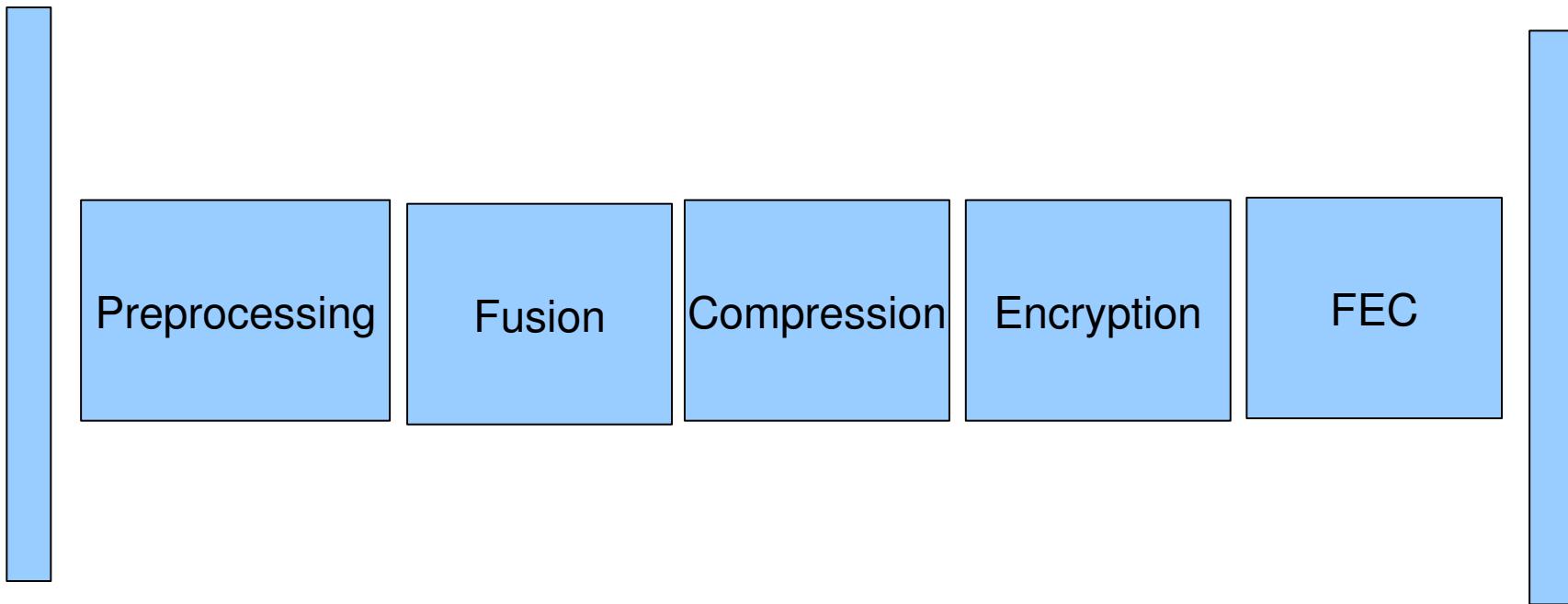
- Reduce traffic by performing data processing locally – at the *Edge*
- Use In-Network Data Aggregation to balance traffic between nodes
- But this requires longer computations and then larger power consumption on the node....

Example : data compression



- On traditional motes, sending one byte of data wirelessly is equivalent to 3000 processor cycles (TmoteSky) at maximal working frequency
- Very application-specific
- Data compression is not always energy-efficient !
- But reduce traffic / risks of bit flips / retransmission

Proposed architecture



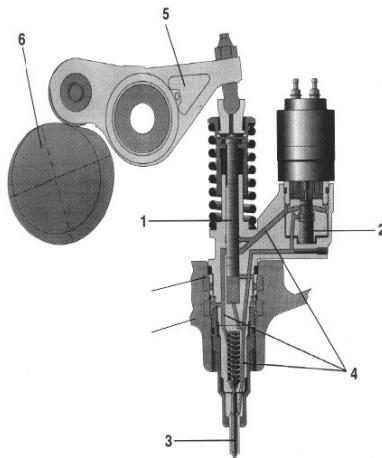
Application to the Adaptronics



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▪ Bridge Health Monitoring :

- Local analysis of the vibrations at different points
- Estimation of the “impulse response” of the bridge
- Health diagnostic
- The estimation of the “impulse response” is executed within the network !



▪ Injector Remaining Useful Lifetime :

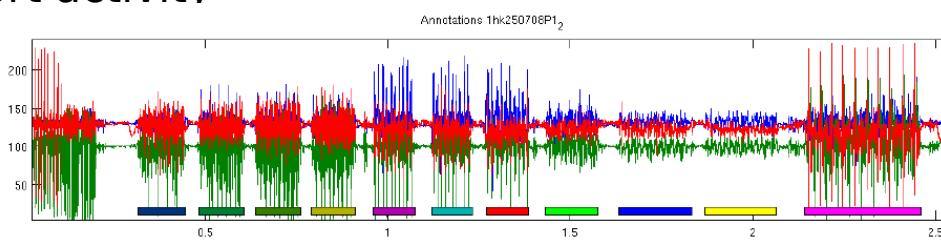
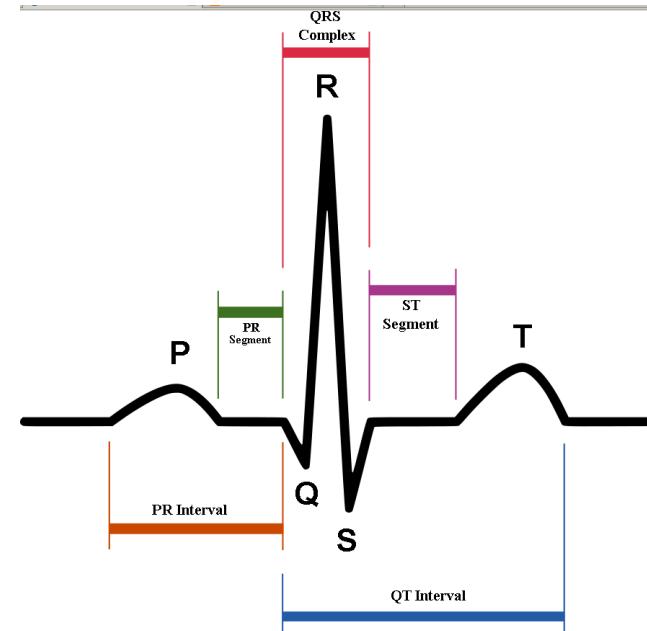
- Measure vibrations with off-the-shell accelerometers
- Detect anomalies or deteriorations
- Forward diagnostic to central unit

Application to Healthcare

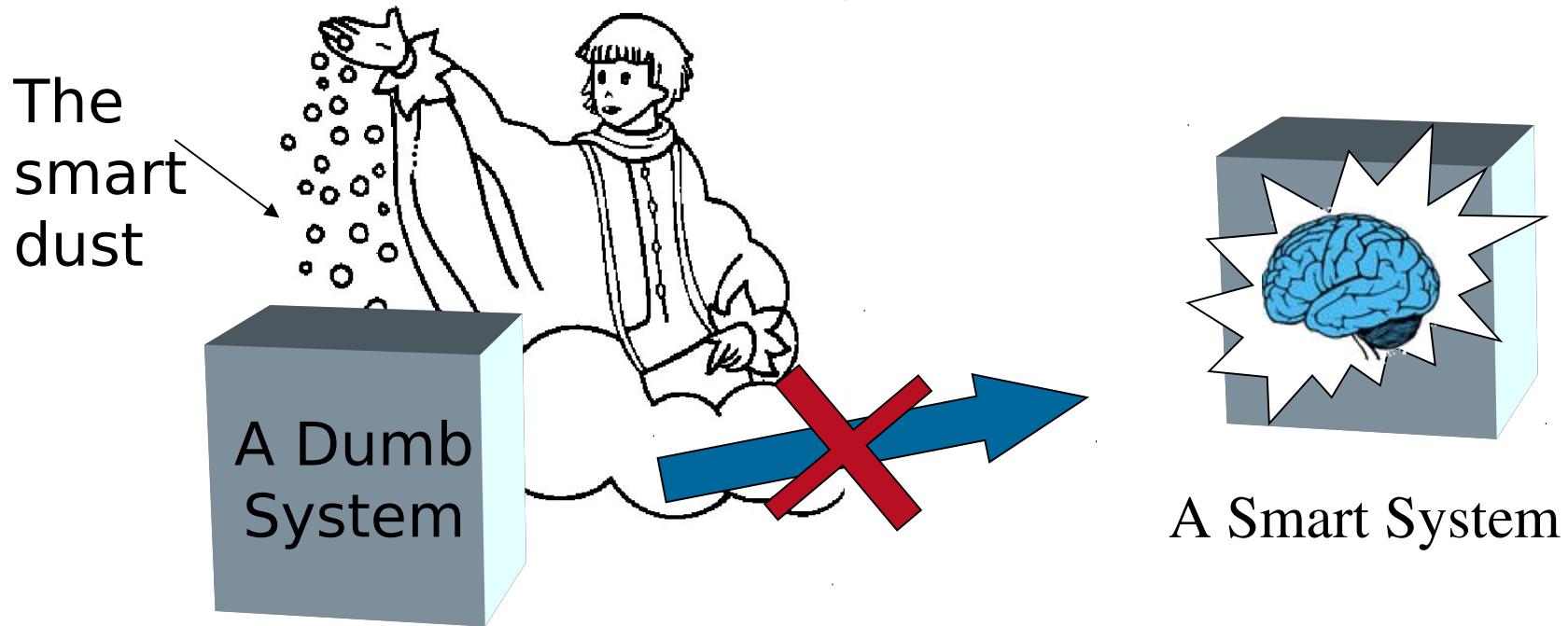


■ Body Area Networks

- Electrocardiogram sensors
- Extract signal features sufficient for further analysis
- Transmit data to patient monitoring station
- Sense moves of a person
- Recognize and classify actions
- Report activity



No Sandman



- Deploying smart sensor networks still requires investigation and design space exploration
- But ultimately, it should be like that

Dependable Wireless Sensor Networks



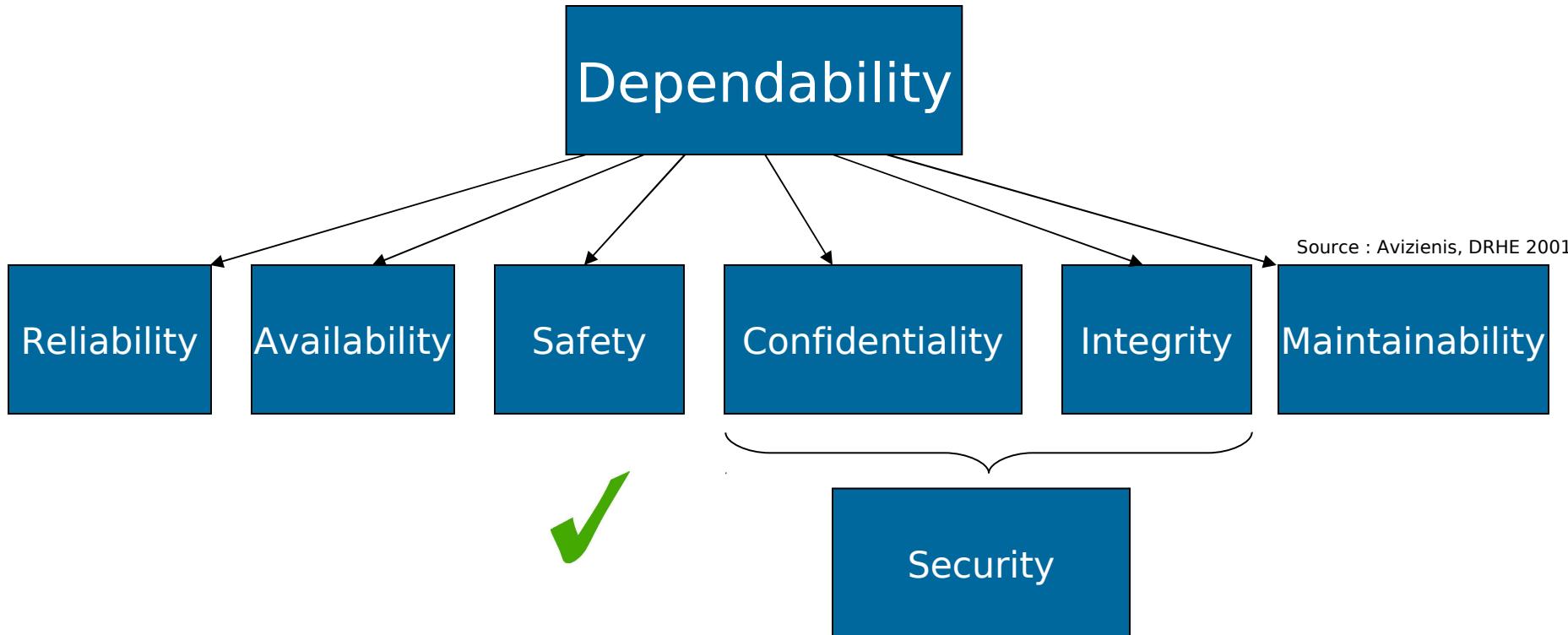
- Computing systems can be characterized by four fundamental properties :

Functionality Performance Cost



- How does our sensor node performs in these areas ?
- Let's have a closer look...

Dependability for WSNs



Availability in WSNs

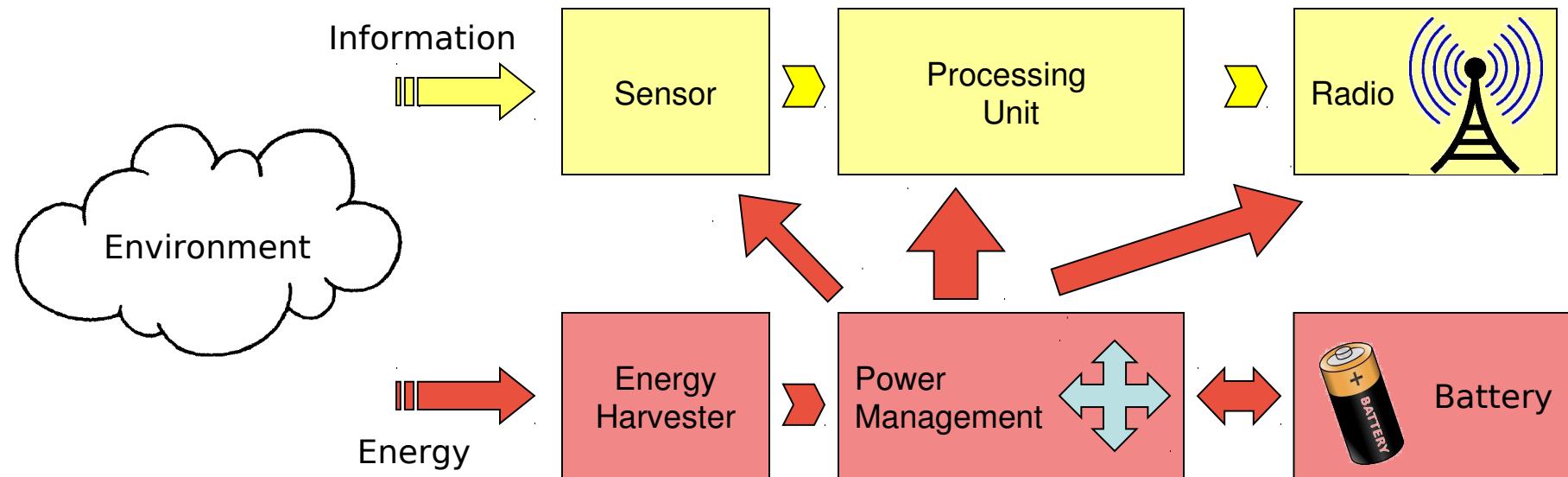


- Nodes should be able to deliver data or to respond to requests
 - as fast as possible
 - as long as possible
- With custom hardware accelerators, nodes are able to deliver data very quickly
 - Faster processing
 - Less traffic
- Lifetime of the network is globally increased, but we can do more...

Towards Zero Energy Motes: Energy Harvesting



- Energy Harvesting enables motes that lives “forever”
- Increase autonomy of the system

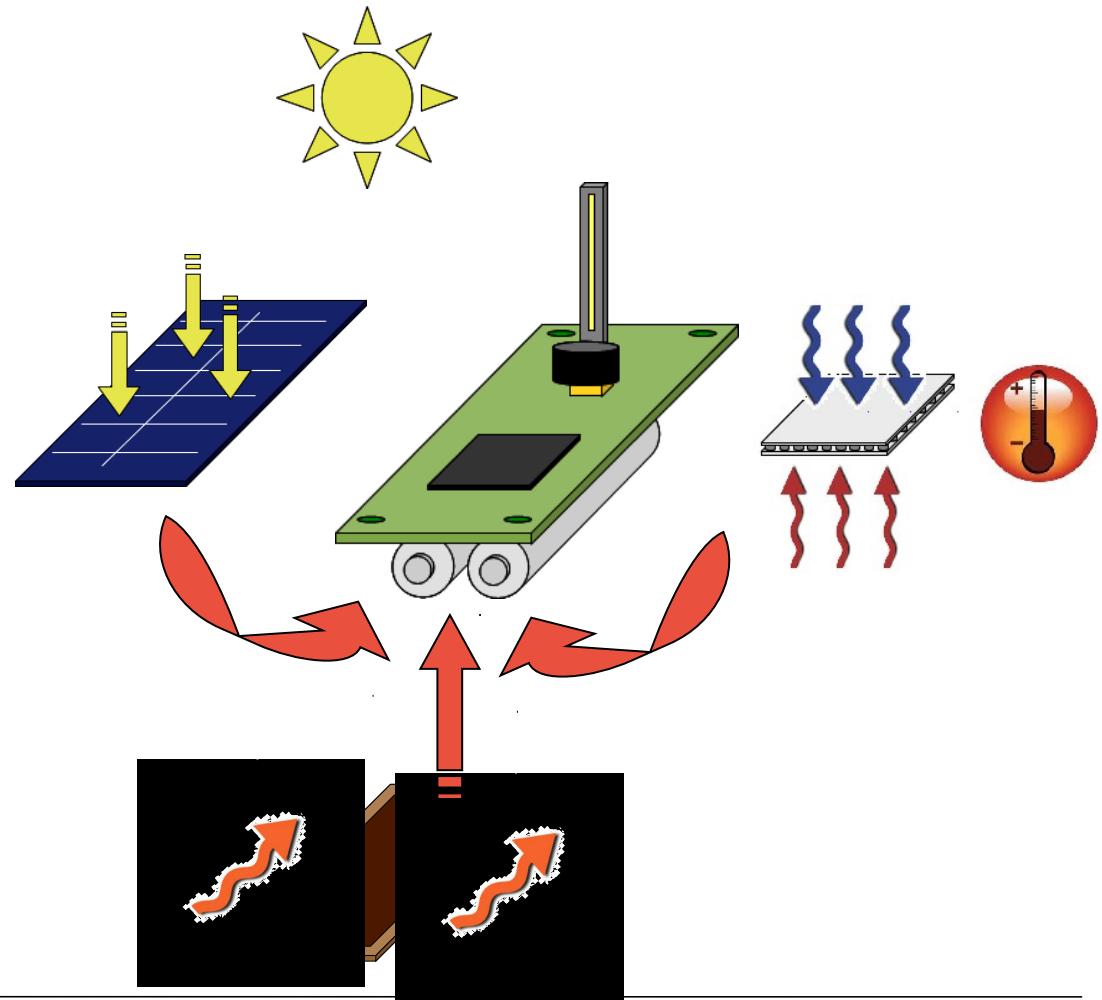


Potential Energy Sources



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- Photovoltaic
 - Light
- Thermogenerator
 - Temperature gradient
- Piezoelectric generator
 - Vibrations



Combination



- Combination energy sources guarantees that energy is available all the time
- Applications :



Vehicles



Wind turbine

Reliable WSNs



- Event-Driven WSNs
- Data-Driven WSNs
- Relevant information has to be routed correctly to the sink
- Low power wireless transmission is not reliable.
 - Many packet losses due to collisions
 - Bit flips lead to packet retransmission
- But...
- Many other kinds of faults could occur...

Failure sources



- Interferences
 - Nodes can not communicate with each other for a long time
 - Lost of synchronization
 - Timeouts, reconstruction of the routing tables
- Node failure
 - Out of Energy
 - Software failure / Crash
 - Detection by timeouts / reconstruction of the routing tables
- Sensor failure
 - Dissemination of erroneous data
 - Lead to wrong results and wrong event detection

Examples



- Critical data for Maintenance on Demand scenario
- Erroneous alerts for patient monitoring
- Detective power consumption report
- For the same reasons, authentication of data is fundamental
- Wireless sensor networks that can not be trust are almost useless



Erroneous Sensor Data



- Sensor node providing erroneous sensor data should NOT be excluded of the network :
 - Still useful for routing
 - May be corrected
- Early detection of erroneous data :
 - Sensor Health monitoring via Hardware
 - Local data pre-analysis
 - Overflows
 - Incoherent values
- Network-wide detection :
 - Incoherent values
 - Avoid propagation

Secure WSNs



- Wireless communication may be easily heared
- Malicious nodes should not be able to join a network
 - Data not routed
 - Insertion of erroneous data
 - → Authentication
- Critical data must be encrypted
 - Additional overhead for processing and communication
- Hardware accelerators provide computational power to reduce this overhead

Maintainability



- Sensor networks are expected to work as long as possible without maintenance
- But after some years, you may want to change some functionality
- Software dynamic reconfiguration is supported by WSN but at high costs :
 - Large data sets requiring high reliability / security
- Using reconfigurable hardware allows hardware dynamic reconfiguration
 - But too large bitstreams
- Coarse-grained reconfigurable hardware ?

Fault Tolerance

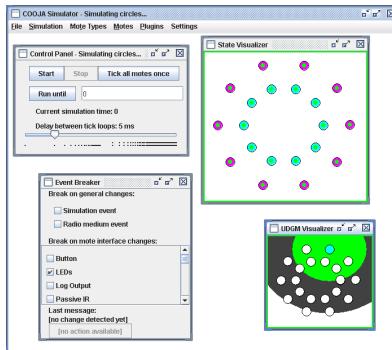


- While developing a wireless sensor network application, fault-tolerance has to be tested and evaluated
- Simulation of interferences and large error rates
- Nodes failures should be simulated
 - Test of adaptive routing algorithms
- Acceptable threshold of failure should be set

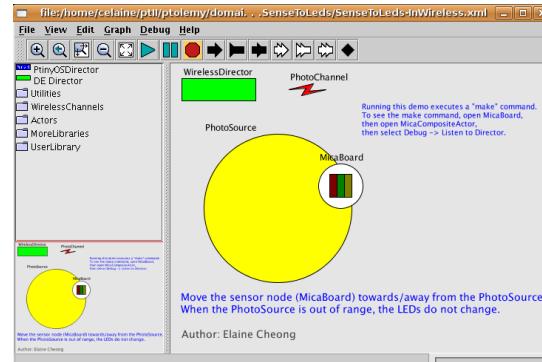
Simulation



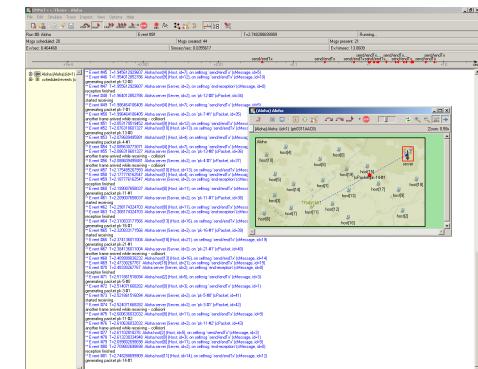
- Behaviour of WSN is highly sensitive to environment
- Simulation and test of WSN is necessary
- Requires accurate models
 - of the Hardware behaviour
 - of the communication
 - of the power consumption
- Today's well known simulators :



Cooja / Contiki



Viptos / TinyOS

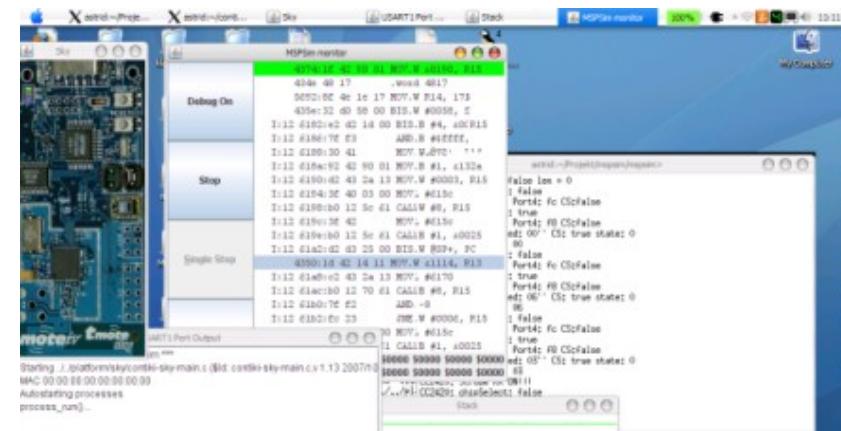


Omnet++

More Accurate Simulations



- MSPSIM
 - Instruction Level Simulator for TmoteSky Motes in Java
- HDL Models
- Gate Level Simulation for very accurate power consumption estimations



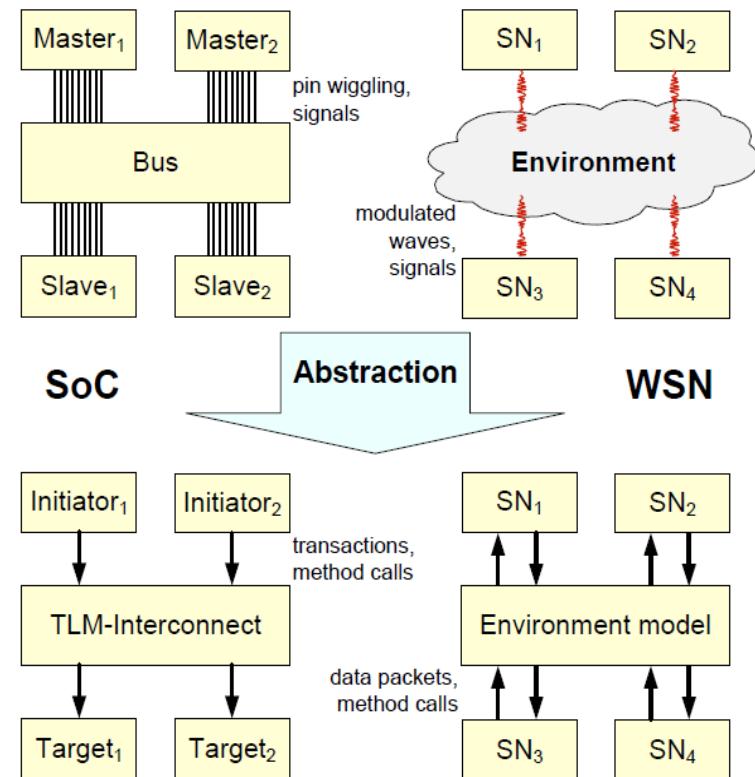
Source : Contiki

Longer Simulations...
No support to simulate large networks...

A trade-off ?



- HW/SW Cosimulation with SystemC
- Instruction Set Simulator
- Transaction-Level Modelling of communication
- Enables development and test of custom hardware while considering a whole network
- Similar abstractions as a SoC design



Conclusions



- Extending motes with custom accelerators implemented on reconfigurable hardware
- Enabling Smart Sensor Networks with high-bandwidth sensing
- Dependable WSNs involves many design challenges

Contact



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The end



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Thank you for your attention !